CHAPTER 5

MOS Field-Effect Transistors (MOSFETs)

Outline

- 5.1 Device structure and physical operation
- 14.1 CMOS Logic-Gate Circuits
- 5.2 $i_D - v_{DS}$ characteristics
- 5.3 MOSFET circuit at DC

5.1 Device structure and physical operation

- 5.1.1 Device structure
  - Metal-Oxide-Semiconductor FET-> MOSFET FET?
  - Three terminals: source, drain, gate, (substrate)
  - Channel region: L (0.03um−1um), W (0.05um−100um)

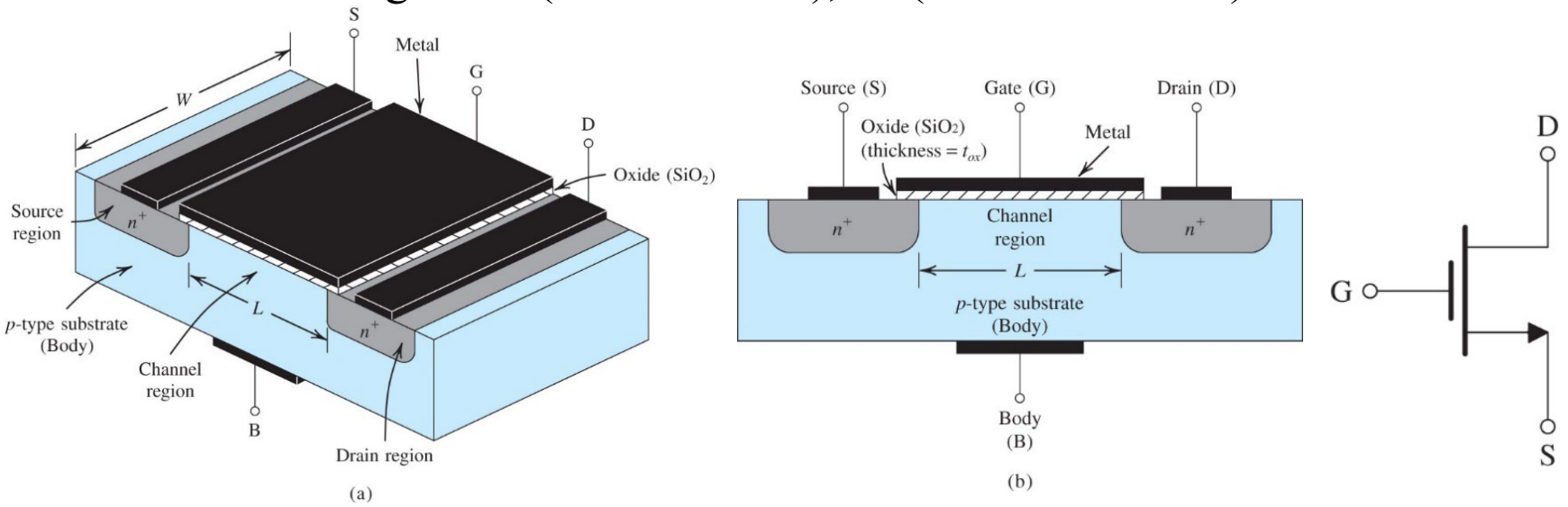


Figure 5.1 Physical structure of the enhancement-type NMOS transistor: **(a)** perspective view; **(b)** cross section. Typically L = 0.03 μm to 1 μm, W = 0.05 μm to 100 μm, and the thickness of the oxide layer (t_{ox}) is in the range of 1 to 10 nm.

- 5.1.3 Field-effect transistor (FET)
  - Positive gate: repel holes and attract electrons from drain and source into the channel
  - Threshold voltage (V_t, 0.3V~1.0V): the value of V_{GS} to form a conducting channel
  - Electric field:
    - Positive on the gate and negative in the channel form a field
    - The filed determines the channel conductivity and the current flow through the channel

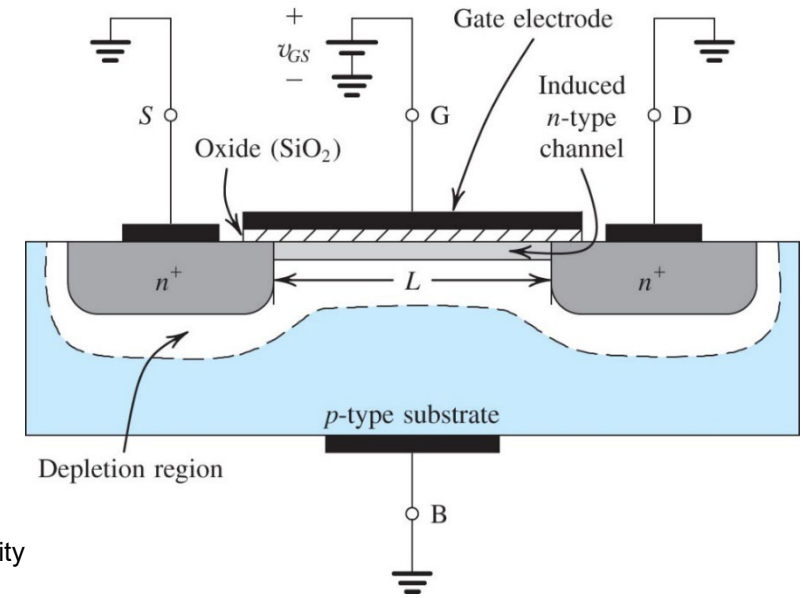


Figure 5.2 The enhancement-type NMOS transistor with a positive voltage applied to the gate. An *n* channel is induced at the top of the substrate beneath the gate.

- 5.1.4 A small v_{DS}: $i_D = [(u_n C_{ox})(\frac{W}{L})(v_{GS} - V_{tn})]v_{DS}$

=> $i_D = k_n v_{oV} v_{DS}$

  - Conductance $g_{DS} = (u_n C_{ox})(\frac{W}{L})(v_{GS} - V_{tn})$
  - $k_n' = u_n C_{ox}$: process transconductance
    - u_n: mobility of the electrons;
    - C_{ox}: oxide capacitance
  - $k_n = k_n' \left(\frac{W}{L}\right)$: MOSFET transconductance
  - $v_{OV} = v_{GS} - V_{tn}$:

    overdrive voltage -- determine the charge of the channel

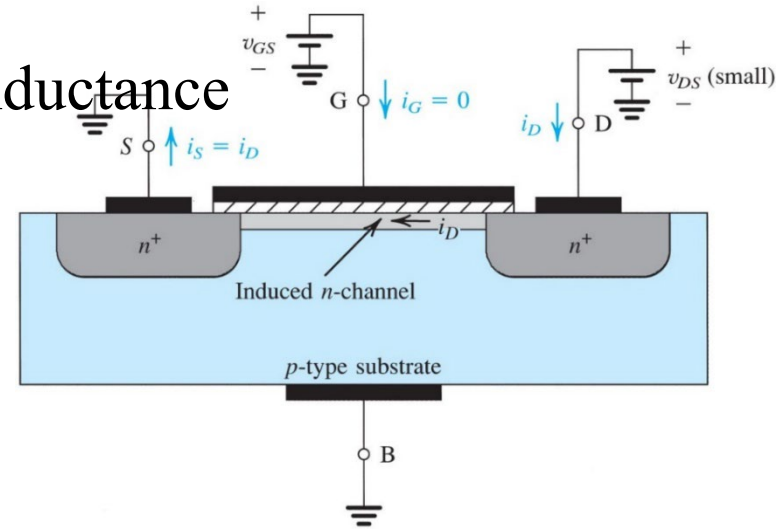


Figure 5.3 An NMOS transistor with $v_{GS} > V_t$ and with a small v_{DS} applied. The device acts as a resistance whose value is determined by v_{GS}. Specifically, the channel conductance is proportional to $v_{GS} - V_t$, and thus i_D is proportional to $(v_{GS} - V_t)v_{DS}$. Note that the depletion region is not shown (for simplicity).

- 5.1.5 v_{DS} increased but $v_{DS} < V_{OV}$:

  $i_D = k'_n \left(\frac{W}{L}\right)\left[(v_{GS} - V_{tn}) - \frac{1}{2}v_{DS}\right]v_{DS}$ => $i_D = k_n(v_{OV} - \frac{1}{2}v_{DS})v_{DS}$

  – Tapered shape channel: deep at source (proportional to V_{OV}) and shallow at drain (proportional to $V_{OV} - v_{DS}$)

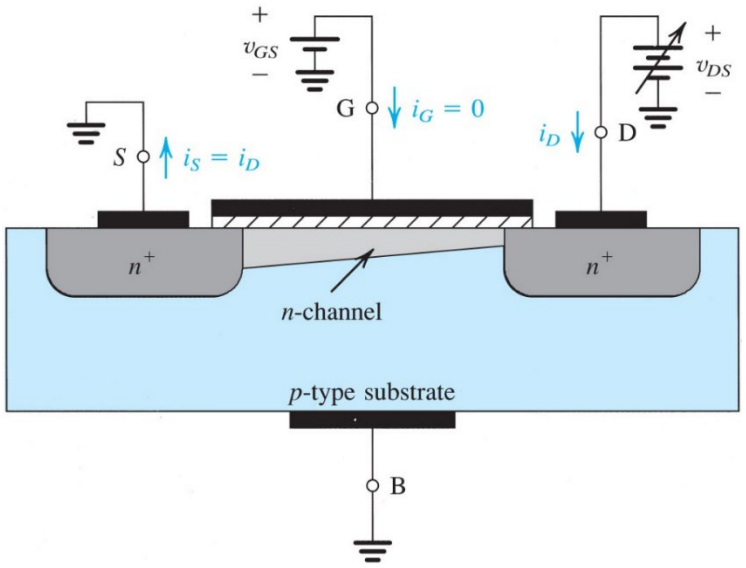


Figure 5.5 Operation of the enhancement-type NMOS transistor as v_{DS} is increased. The induced channel acquires a tapered shape, and its resistance increases as v_{DS} is increased. Here, v_{GS} is kept constant at a value > V_t; $v_{GS} = V_t + V_{OV}$.

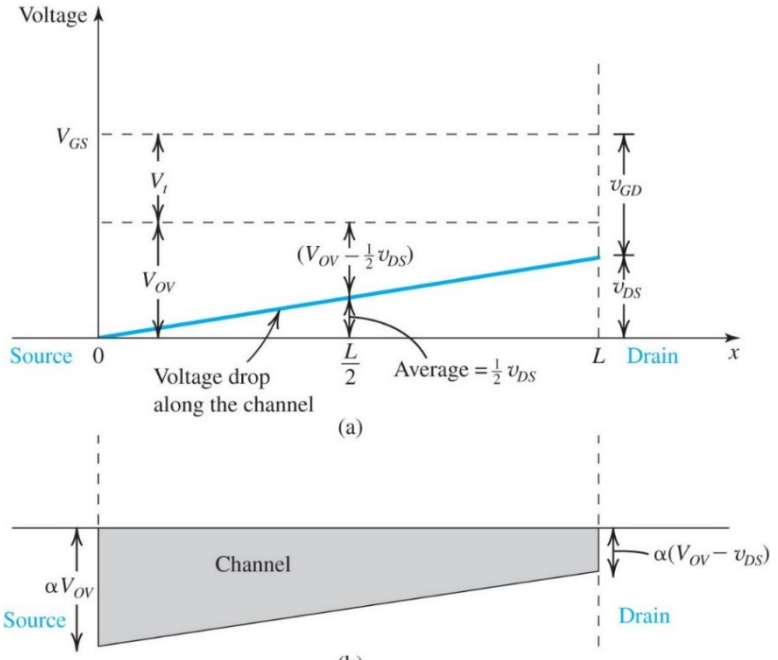


Figure 5.6 (a) For a MOSFET with $v_{GS} = V_t + V_{OV}$, application of v_{DS} causes the voltage drop along the channel to vary linearly, with an average value of $\frac{1}{2}v_{DS}$ at the midpoint. Since $v_{DS} > V_t$, the channel still exists at the drain end. (b) the channel shape corresponding to the situation in (a). While the depth of the channel at the source end is still proportional to V_{OV}, that at the drain end is proportional to $V_{OV} - v_{DS}$

- 5.1.6 $v_{DS} \geq V_{OV}$: channel pinch-off and current saturation, $i_D = \frac{1}{2} k_n' \left(\frac{W}{L}\right) (v_{GS} - V_{tn})^2$

=> $i_D = \frac{1}{2} k_n {v_{OV}}^2$

  – Current remains constant

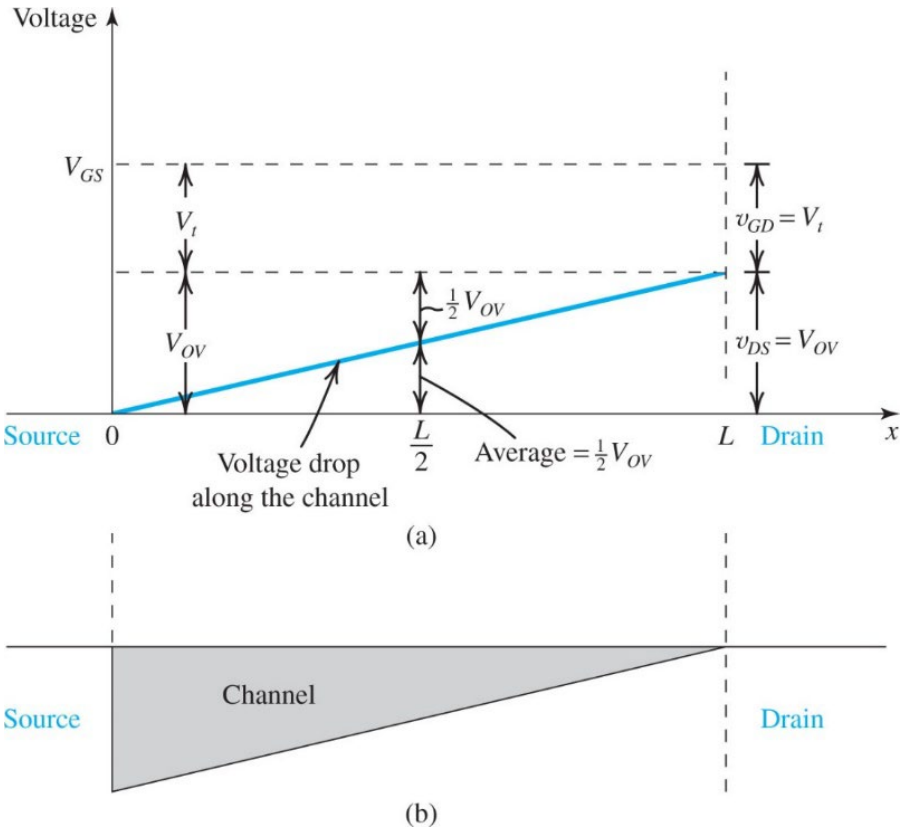


Figure 5.8 Operation of MOSFET with $v_{GS} = V_t + V_{OV}$, as v_{DS} is increased to V_{OV}. At the drain end, v_{GD} decreases to V_t and the channel depth at the drain end reduces to zero (pinch-off). At this point, the MOSFET enters the saturation mode of operation. Further increasing v_{DS} (beyond $V_{DSsat} = V_{OV}$) has no effect on the channel shape and i_D remains constant.

- Conclution:
  - $v_{GS} < V_{tn}$: cut off
  - $v_{GS} > V_{tn}$: channel conducted
    - A small v_{DS}: $i_D = k_n v_{oV} v_{DS}$
    - v_{DS} increased: $i_D = k_n(v_{oV} - \frac{1}{2} v_{DS}) v_{DS}$
    - $v_{DS} \geq V_{OV}$: channel pinch-off and current saturation

      $i_D = \frac{1}{2} k_n {v_{OV}}^2$

$$k_n' = u_n C_{ox}\,, k_n = k_n' \left(\frac{W}{L}\right), v_{OV} = v_{GS} - V_{tn}$$

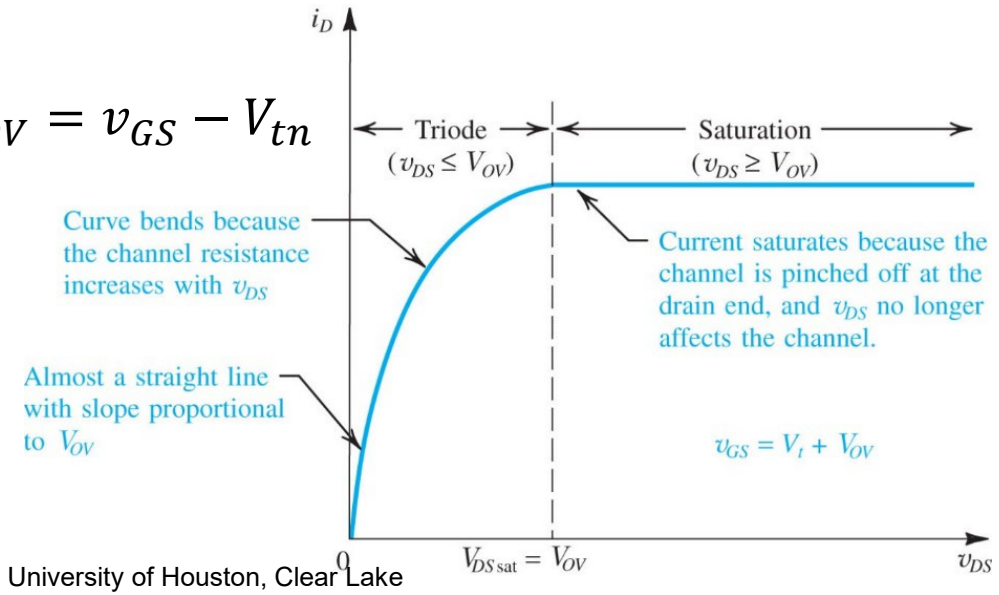


Figure 5.7 the drain current i_D versus the drain-to-source voltage v_{DS} for an enhancement-type NMOS transistor operated with $v_{GS} = V_t + V_{OV}$.

- # Example 5.1

Consider a process technology for which $L = 0.4um$, $C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} = 4.32 \times 10^{-3}\,\frac{F}{m^2}$ $(hint:\ F = \frac{A \cdot S}{V})$, $u_n = 450\,\frac{cm^2}{V \cdot s}$, and $V_{tn} = 0.7V$.

(a) Find process transconductance k_n'

(b) For $\frac{W}{L} = \frac{8um}{0.8um}$, calculate $V_{OV}, V_{GS}, V_{DSmin}$ needed to operate the transistor in saturation region with a dc current $I_D = 100uA$

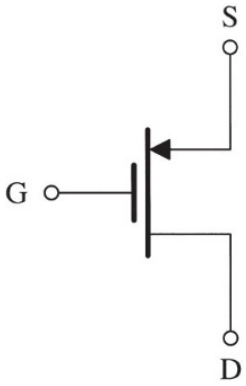
(a) $k_n' = u_n C_{ox} = 4.32 \times 10^{-3}\,\frac{F}{m^2} \times 450\,\frac{cm^2}{V \cdot s} = 4.32 \times 10^{-3}\,\frac{A \cdot s}{V \cdot m^2} \times 450 \times 10^{-4}\,\frac{m^2}{V \cdot s} = 1944 \times 10^{-7}\,\frac{A}{V^2} = 194.4\,\frac{uA}{V^2}$

(b) In saturation region, $i_D = \frac{1}{2} k_n' \left(\frac{W}{L}\right) V_{OV}^2 \quad (Hint: V_{OV} = V_{GS} - V_{tn})$

$$V_{OV} = \sqrt{\frac{2 i_D}{k_n' \left(\frac{W}{L}\right)}} = 0.32V \qquad V_{GS} = V_t + V_{OV} = 1.02V$$

At the edge of saturation and triode, $V_{DSmin} = V_{OV} = 0.32V$

- 5.1.7 PMOS: P-Channel MOSFET
  - $V_{SG} \geq |V_{tP}|$
  - $k'_p = u_p C_{ox}$
    - u_p is mobility of the holes
    - $u_p = 0.25u_n \; to \; 0.5u_n$



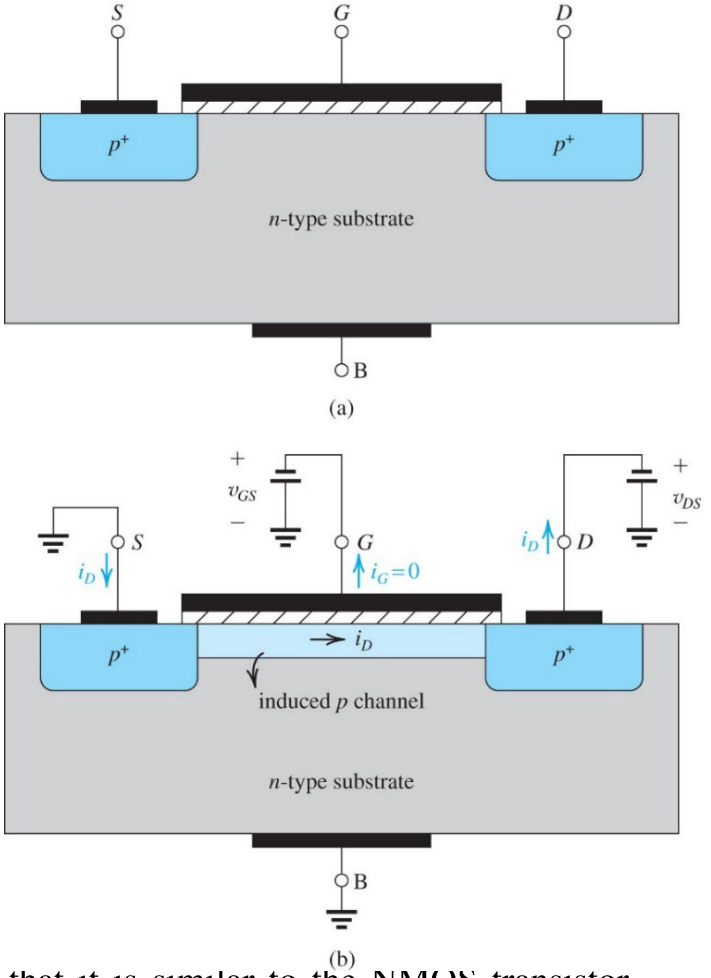


Figure 5.9 **(a)** Physical structure of the PMOS transistor. Note that it is similar to the NMOS transistor shown in Fig. 5.1(b) except that all semiconductor regions are reversed in polarity. **(b)** A negative voltage v_{GS} of magnitude greater than V_{tp} induces a *p* channel, and a negative v^{DS} causes a current i^D to flow from source to drain.

- Conclusion for PMOS:
  - $v_{SG} < |V_{tp}|$: cut off
  - $v_{SG} > |V_{tp}|$: channel conducted
    - A small v_{SD}: $i_D = k_p v_{oV} v_{SD}$
    - v_{SD} increased: $i_D = k_p(v_{oV} - \frac{1}{2} v_{SD}) v_{SD}$
    - $v_{SD} \geq V_{OV}$: channel pinch-off and current saturation

      $i_D = \frac{1}{2} k_p {v_{OV}}^2$

$$k_p' = u_p C_{ox}\,, k_p = k_p' \left(\frac{W}{L}\right), v_{OV} = v_{SG} - |V_{tp}|$$

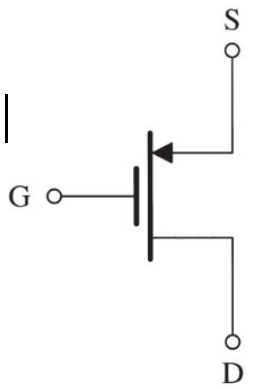


Figure 5.7 the drain current i_D versus the drain-to-source voltage v_{SD} for an enhancement-type PMOS transistor operated with $v_{SG} = V_{tp} + V_{OV}$.

- # Example 5.2

For a $0.18\text{-}um$ fabrication process with $W = 2um$. The process is specified to have $C_{ox} = 8.6\frac{fF}{um^2}, \left(hint: 1fF = 10^{-15}F, F = \frac{A \cdot S}{V}\right), u_n = 450cm^2/V \cdot s,$ and $V_{tn} = 0.5V$.

(a) Find V_{GS} and V_{DS} that result in the MOSFET operating at the edge of saturation with $I_D = 100uA$.

$$k_n' = u_n C_{ox} = 450 \times 10^8 \frac{um^2}{V \cdot s} \times 8.6 \times 10^{-15} \frac{F}{um^2} = 387 \frac{uA}{V^2}$$

$$k_n = k_n' \left(\frac{W}{L}\right) = 387 \times \frac{2}{0.18} = 4.3 \times 10^3 \frac{uA}{V^2}$$

(a) At the edge of saturation, $I_D = \frac{1}{2} k_n {V_{ov}}^2$,

$100 = \frac{1}{2} \times 4.3 \times 10^3 \times {V_{ov}}^2$, => $V_{OV} = 0.22V$

Thus $V_{DS} = V_{OV} = 0.22V$ and $V_{GS} = V_{OV} + V_{tn} = 0.72V$

- Example 5.2

For a $0.18\text{-}um$ fabrication process with $W = 2um$. The process is specified to have $C_{ox} = 8.6\frac{fF}{um^2}, (hint: 1fF = 10^{-15}F), u_n = 450cm^2/V \cdot s$, and $V_{tn} = 0.5V$.

(b) If V_{GS} is kept constant, find V_{DS} that result in $I_D = 50uA$.

(b) With $V_{GS} = 0.72V$ and I_D reduced from the value obtained at the edge of saturation ($I_D = 100uA$), the MOSFET will be working in triode region.

In triode region, $I_D = k_n\,(V_{OV} - \frac{1}{2}V_{DS})V_{DS}$,

$50 = 4.3 \times 10^3 \times (0.22 - \frac{1}{2}V_{DS})V_{DS}$,

$\Rightarrow V_{DS}^2 - 0.44V_{DS} + 0.023 = 0$

Thus $V_{DS} = 0.06V$ and $V_{DS} = 0.39V$

If $V_{DS} = 0.39V$, the transistor is in saturation region, so $V_{DS} = 0.06V$

- 5.2.4 Finite output resistance in saturation
  - Channel-length modulation
    - As v_{DS} increases, the channel pinch-off point is moved slightly away from the drain, toward the source (channel length reduced).
    - i_D is inversely proportional to channel length, so increases with v_{DS}
  - $i_D = \frac{1}{2} k'_n \left(\frac{W}{L}\right)(V_{GS} - V_{tn})^2 (1 + \lambda v_{DS})$
    - λ: device parameter with unit of reciprocal volts (V^{-1})
    - $V_A = \frac{1}{\lambda}$, early voltage (J. M. Early discovered)

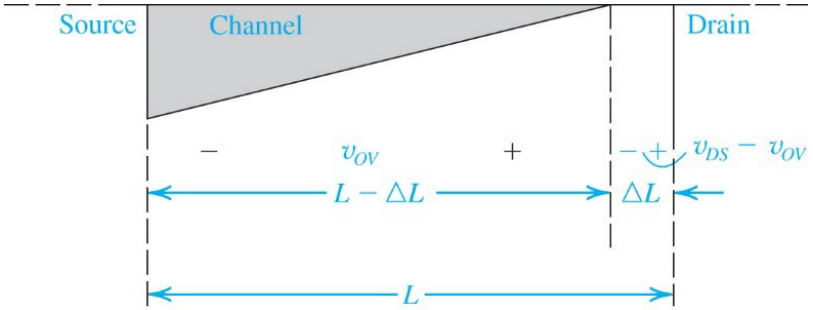


Figure 5.16 Increasing v_{DS} beyond v_{DSsat} causes the channel pinch-off point is moved slightly away from the drain, thus reducing the effective channel length (by ΔL).

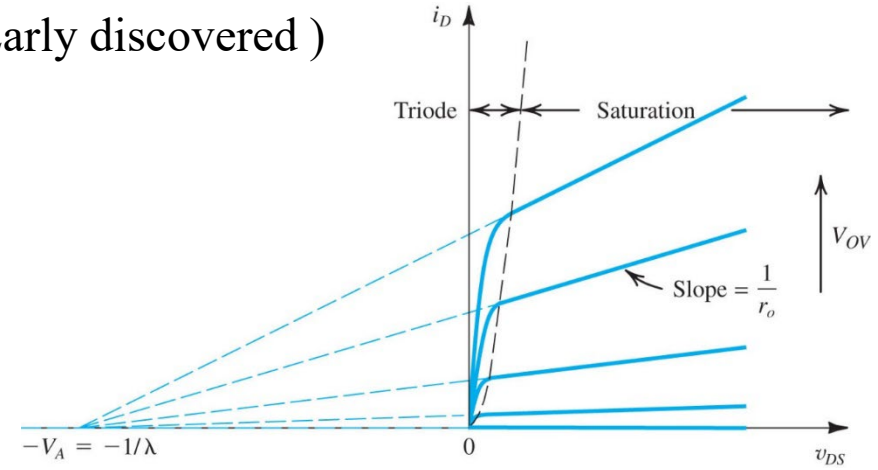
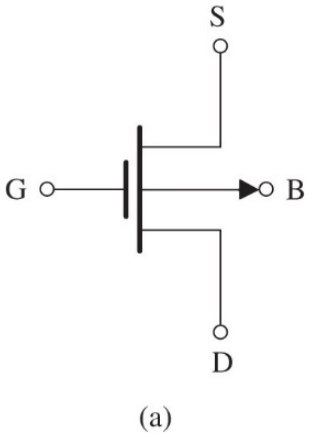


Figure 5.16 Effect of v_{DS} on i_D in the saturation region. The MOSFET parameter V_A depends on the process technology and, for a given process, is proportional to the channel length L.

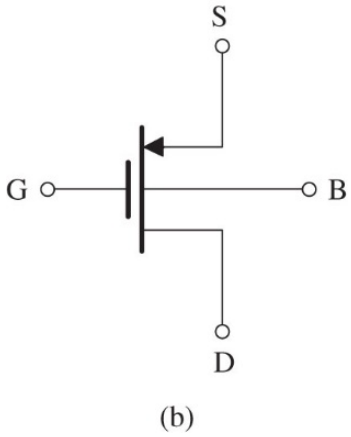
- 5.2.5 P-channel MOSFET symbols and characteristics

$$I_D = \frac{1}{2} k'_p \left(\frac{W}{L}\right) (V_{SG} - |V_{tp}|)^2 (1 + |\lambda| V_{SD})$$



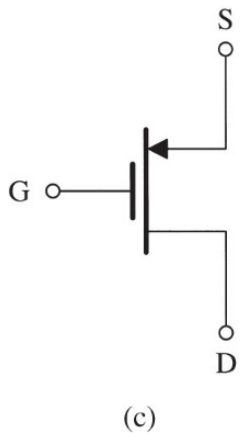
(a)

Figure 5.19 (a) Circuit symbol for the *p*-channel enhancement-type MOSFET.



(b)

Figure 5.19 (b) Modified symbol with an arrowhead on the source lead.



(c)

Figure 5.19 (c) Simplified circuit symbol for the case where the source is connected to the body.

- 14.1.1 Switch-level Transistor Model
  - NMOS:
    - Behaves as a closed switch when its gate is “high”
    - Conversely when the gate is low the transistor is cut off.
  - PMOS:
    - Complementary fashion

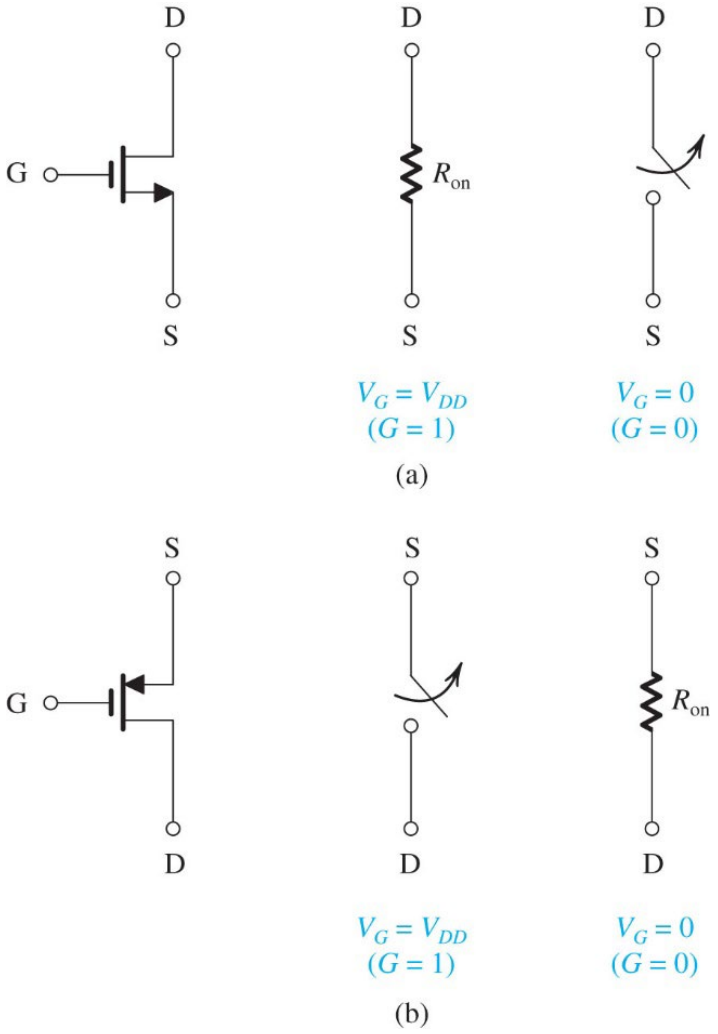


Figure 14.1 Operation of the (**a**) NMOS and (**b**) PMOS transistor as an on/off switch. The gate voltage controls the operation of the transistor switch, with the voltage V_{DD} representing a logic 1 and 0 V representing a logic 0. Note that the connections of the drain and source terminals are not shown.

- 14.1.2 The CMOS Inverter
  - $Y = \overline{X}$

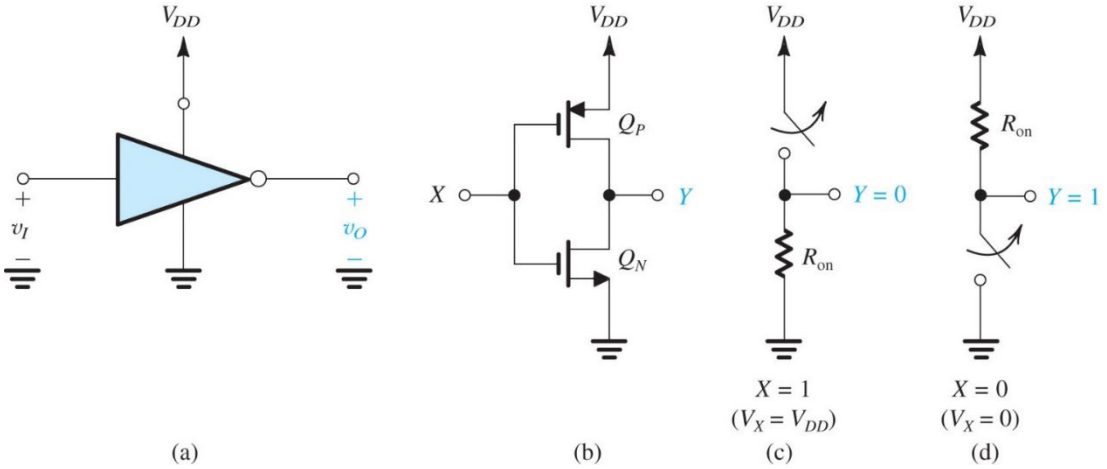


Figure 14.2 (**a**) Block representation of the logic inverter; (**b**) its CMOS realization; (**c**) operation when the input is a logic 1; (**d**) operation when the input is a logic 0.

- 14.1.3 General Structure of CMOS Logic
  - NMOS pull-down transistor
  - PMOS pull-up transistor

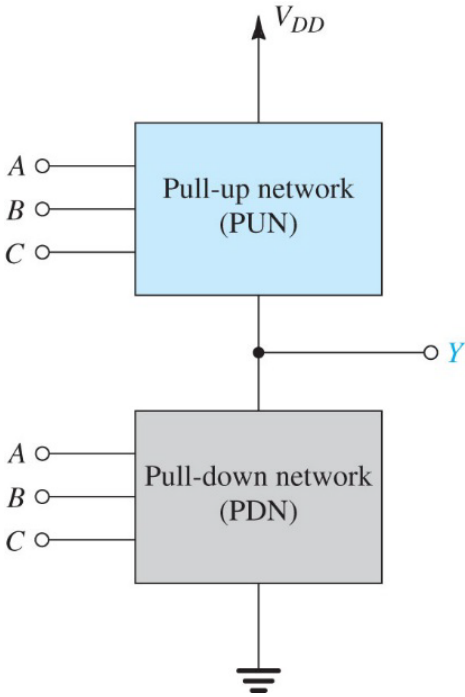


Figure 14.3 Representation of a three-input CMOS logic gate. The PUN comprises PMOS transistors, and the PDN comprises NMOS transistors.

- 14.1.3 General Structure of CMOS Logic

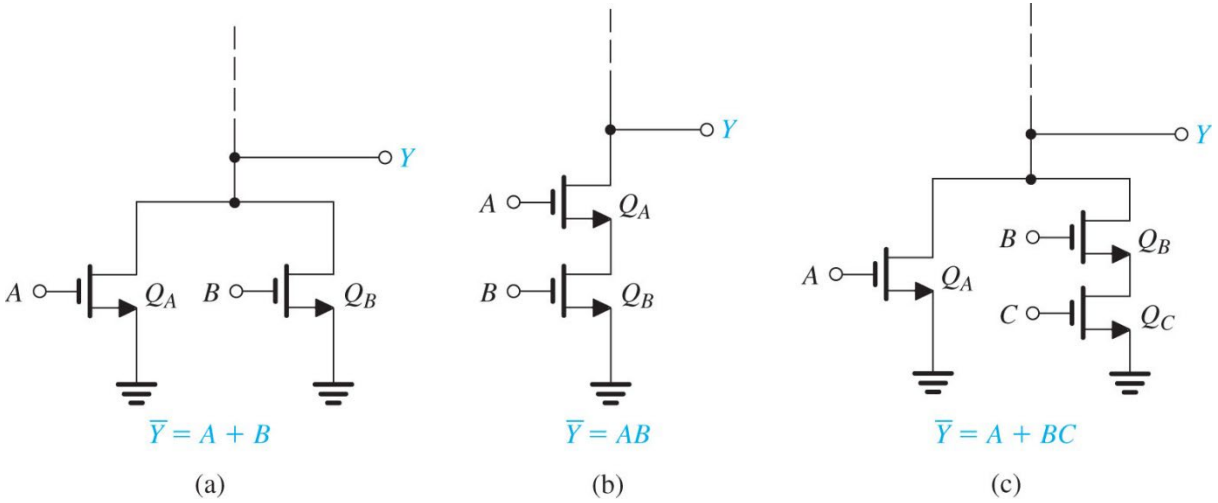


Figure 14.4 Examples of pull-down networks.

Y NOT:
Parallel network -> OR
Series network -> AND

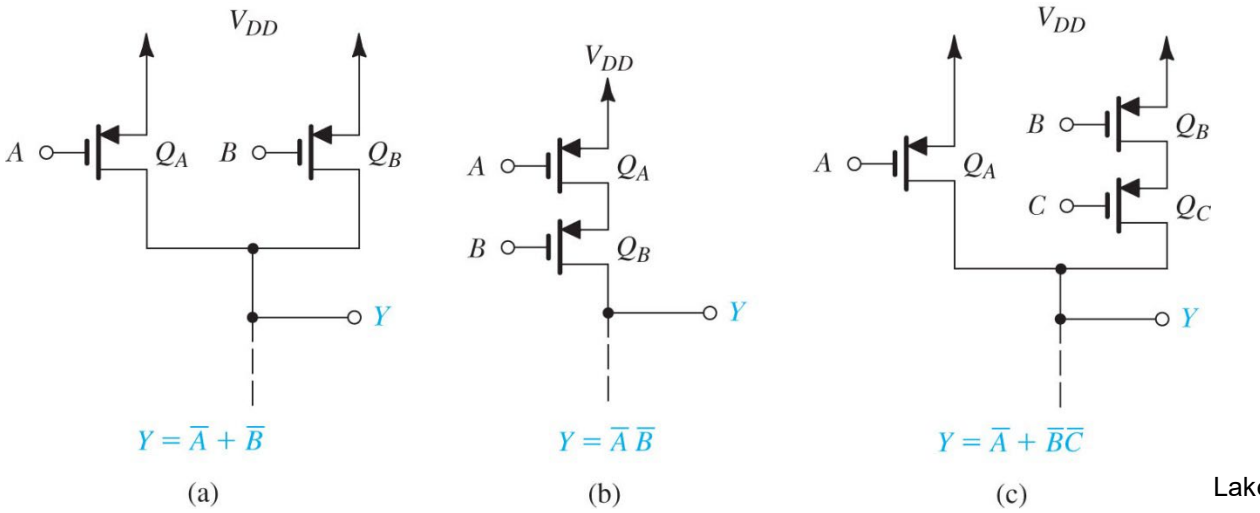


Figure 14.5 Examples of pull-up networks.

Y:
Parallel network -> NOT OR
Series network -> NOT AND

- 14.1.4-5 The Tow-Input NOR and NAND Gates

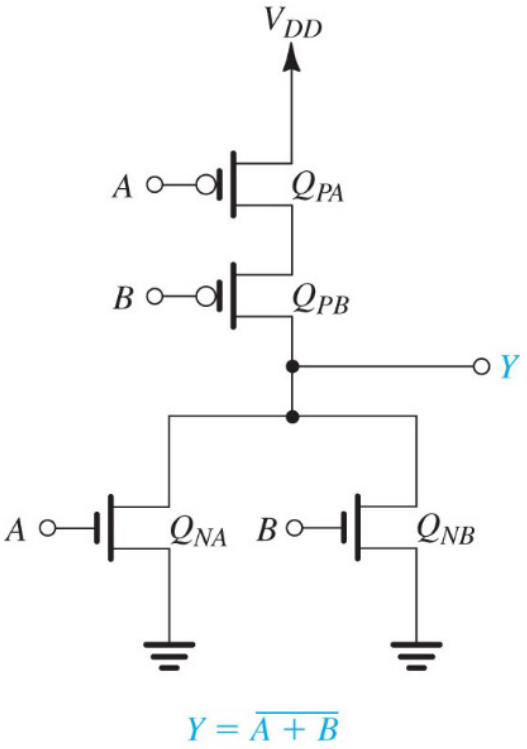


Figure 14.7 A two-input CMOS NOR gate.

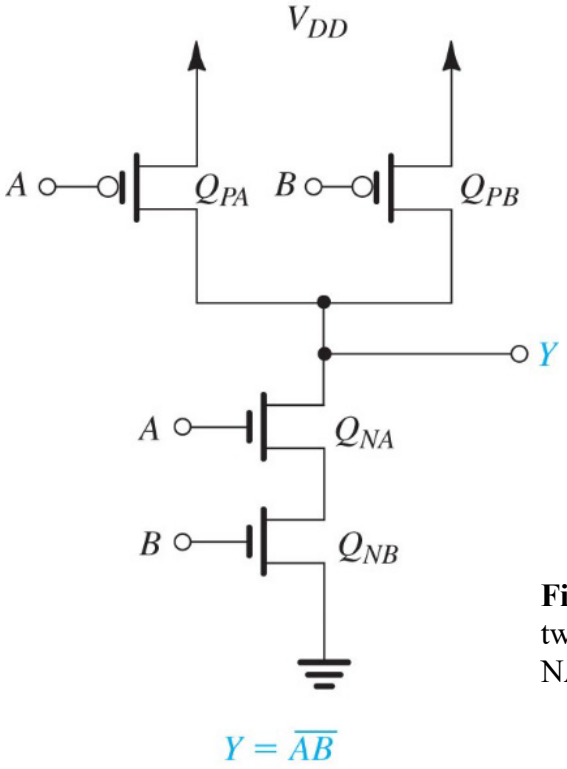


Figure 14.8 A two-input CMOS NAND gate.

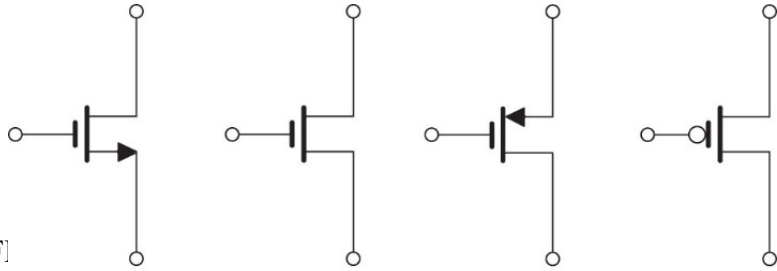


Figure 14.6 Usual and alternative circuit symbols for MOSF

- 14.1.6-7 A Complex Gate and Exclusive-OR Function

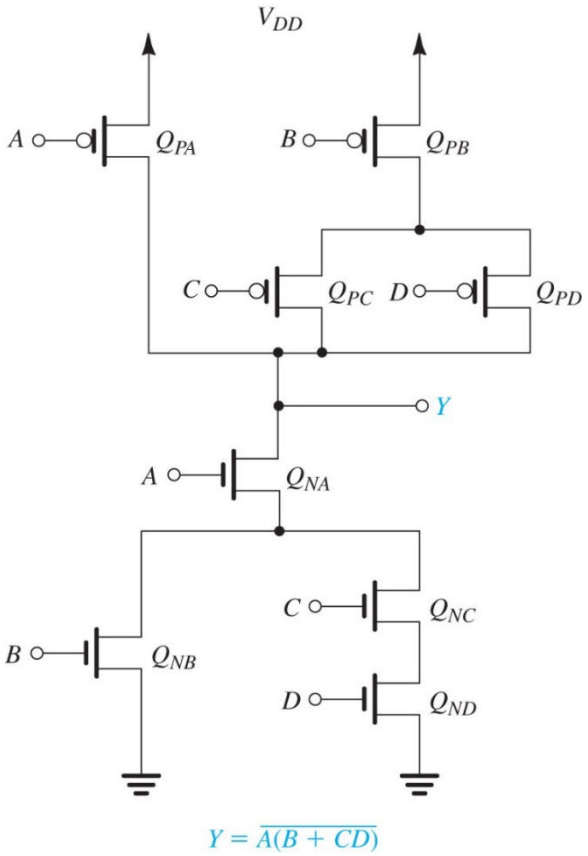


Figure 14.9 CMOS realization of a complex gate.

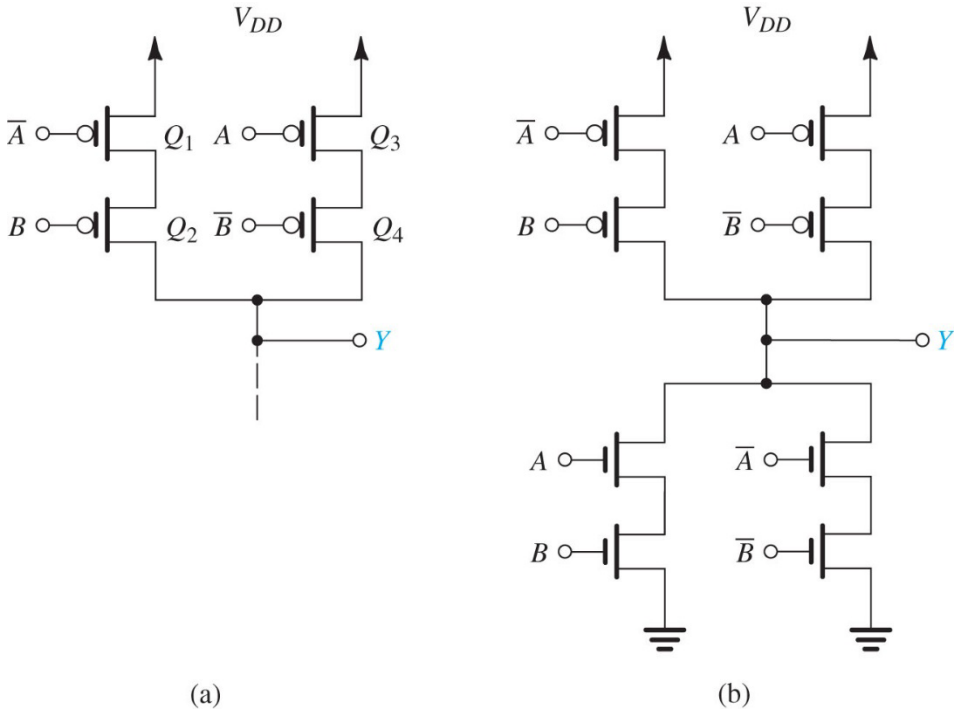


Figure 14.10 Realization of the exclusive-OR (XOR) function. **(a)** The PUN synthesized directly from the expression in Eq. (14.5). **(b)** The complete XOR realization utilizing the PUN in **(a)** and a PDN that is synthesized directly from the expression in Eq. (14.6). Note that two inverters (not shown) are needed to generate the complemented variables. Also note that in this XOR realization, the PDN and the PUN are not dual networks; however, a realization based on dual networks is possible (see Problem 14.9).

- 14.1.8 Example 14.1
- Synthesize a CMOS logic circuit that implements the Boolean function $Y = \overline{A + B(C + D)}$

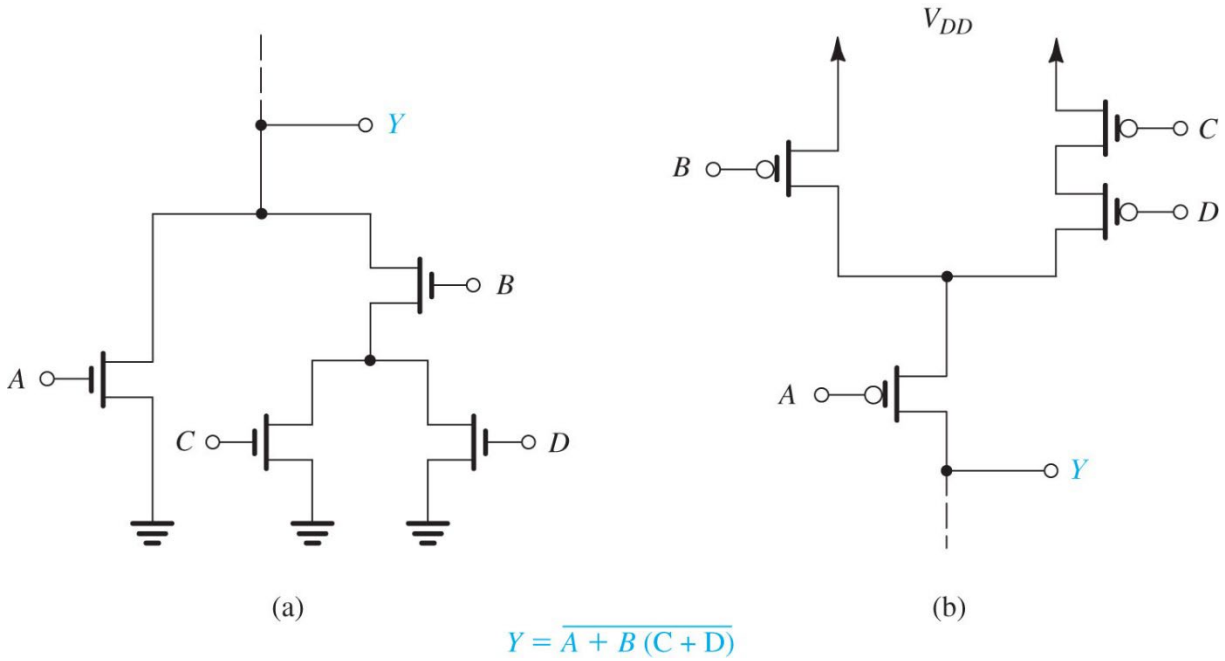
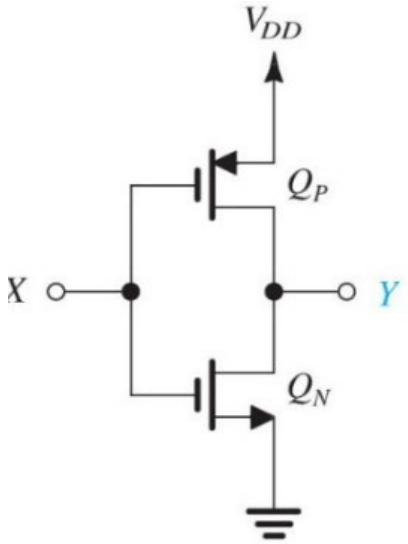


Figure 14.11 (a) The PDN and **(b)** the PUN for the logic function in Example 14.1.

- # Experiment 6.1

Set up the following circuit using nMOSFET and pMOSFET in **Multisim**. $V_{DD} = 5V, Digit\ 1 = 5V, Digit\ 0 = ground/0V$



Multisim simulation results:

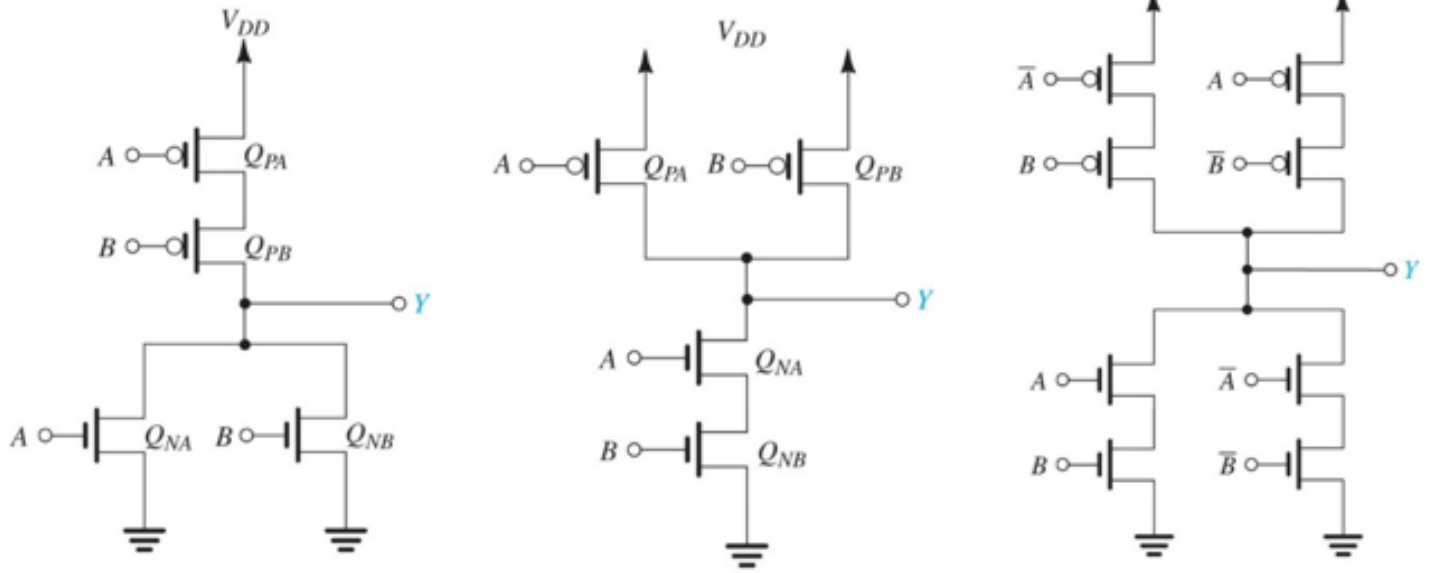
Input X (V)	Output Y (V)
0	
1	

1) Use a multimeter to apply digits 1 and 0 to the input, measure the corresponding output, and record the results in the table below.

2) Provide the Boolean expression and analyze the CMOS logic gate circuit

• Experiment 6.2

Set up the following circuit using nMOSFET and pMOSFET in **Multisim**. $V_{DD} = 5V, Digit\ 1 = 5V, Digit\ 0 = ground/0V$



(a) (b) (c)

1) Use a multimeter to apply digits 1 and 0 to the inputs, measure the corresponding output, and record the results in the table below. 2) Provide the Boolean expressions and analyze the CMOS logic gate circuits

Multisim simulation results of circuits (a)-(c):

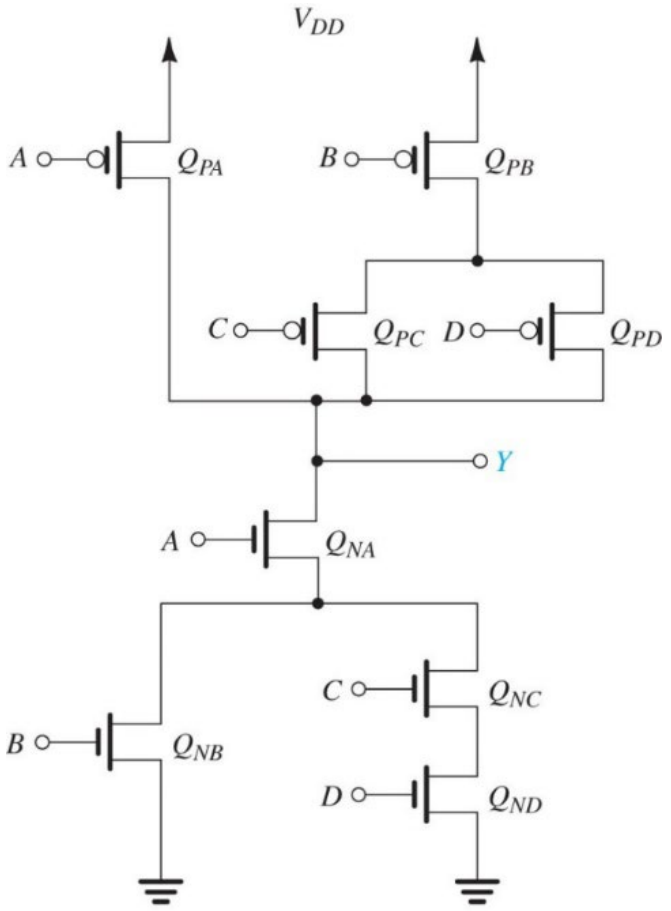
Input A	Input B	Circuit (a) Output Y	Circuit (b) Output Y	Circuit (c) Output Y
0	0			
0	1			
1	0			
1	1			

• Experiment 6.3

Set up the following circuit using nMOSFET and pMOSFET in **Multisim**. $V_{DD} = 5V, Digit\ 1 = 5V, Digit\ 0 = ground/0V$

Multisim simulation results of circuit:

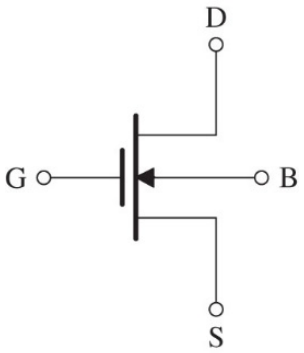
Input A	Input B	Input C	Input D	Output Y
0	0	0	0	
0	0	0	1	
0	0	1	0	
0	0	1	1	
0	1	0	0	
0	1	0	1	
0	1	1	0	
0	1	1	1	
1	0	0	0	
1	0	0	1	
1	0	1	0	
1	0	1	1	
1	1	0	0	
1	1	0	1	
1	1	1	0	
1	1	1	1	



1) Use a multimeter to apply digits 1 and 0 to the inputs, measure the corresponding output, and record the results in the table below. 2) Provide the Boolean expressions and analyze the CMOS logic gate circuits

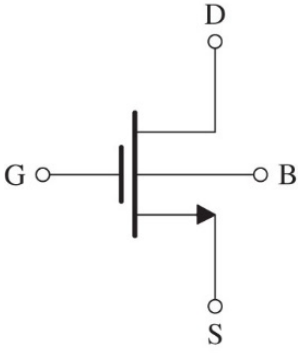
5.2 $i_D - v_{DS}$ characteristics

- 5.2.1 Circuit symbol
  - (a) isolation (spacing between the vertical lines) and polarity (arrowhead)
  - (b) current from drain to source (c) simplified symbol



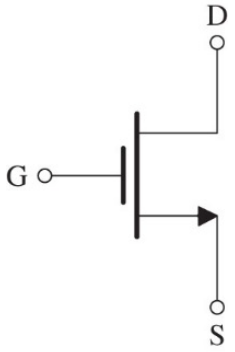
(a)

Figure 5.11 (a) Circuit symbol for the *n*-channel enhancement-type MOSFET



(b)

Figure 5.11 (b) Modified circuit symbol with an arrowhead on the source terminal to distinguish it from the drain and to indicate device polarity (i.e., *n* channel).

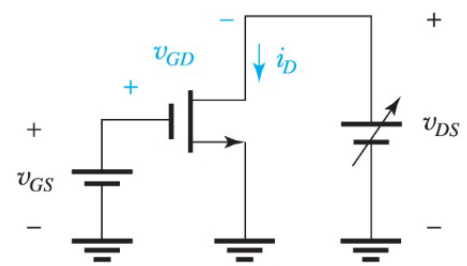


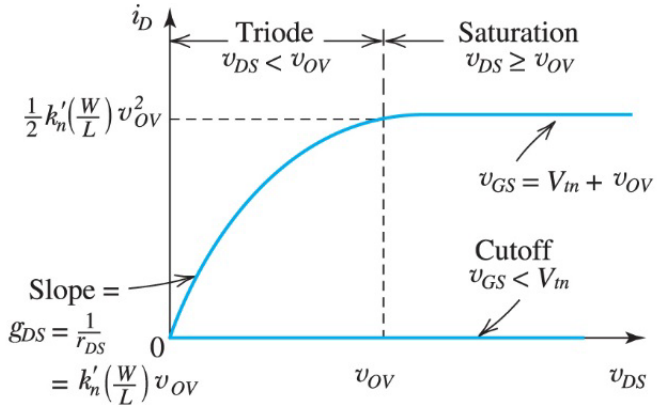
(c)

Figure 5.11 (c) Simplified circuit symbol to be used when the source is connected to the body or when the effect of the body on device operation is unimportant.

• 5.2.2 The NMOS $i_D - v_{DS}$ characteristics

Table 5.1 Regions of Operation of the Enhancement NMOS Transistor





- $v_{GS} < V_{tn}$: no channel; transistor in cutoff; $i_D = 0$
- $v_{GS} = V_{tn} + v_{OV}$: a channel is induced; transistor operates in the triode region or the saturation region depending on whether the channel is continuous or pinched off at the drain end;

Triode Region

Continuous channel, obtained by:

$$v_{GD} > V_{tn}$$

or equivalently:

$$v_{DS} < v_{OV}$$

Then,

$$i_D = k_n'\left(\frac{W}{L}\right)\left[(v_{GS} - V_{tn})v_{DS} - \frac{1}{2}v_{DS}^2\right]$$

or equivalently

$$i_D = k_n'\left(\frac{W}{L}\right)\left(v_{OV} - \frac{1}{2}v_{DS}\right)v_{DS}$$

Saturation Region

Pinched-off channel, obtained by:

$$v_{GD} \leq V_{tn}$$

or equivalently:

$$v_{DS} \geq v_{OV}$$

Then

$$i_D = \frac{1}{2}k_n'\left(\frac{W}{L}\right)(v_{GS} - V_{tn})^2$$

or equivalently

$$i_D = \frac{1}{2}k_n'\left(\frac{W}{L}\right)v_{OV}^2$$

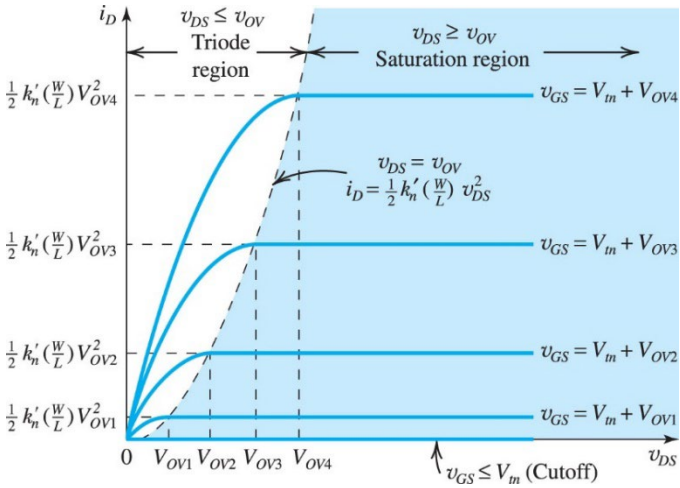
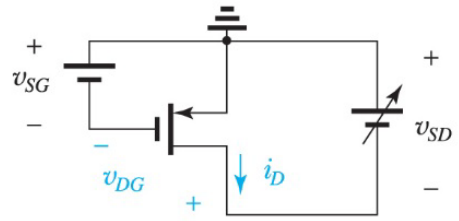
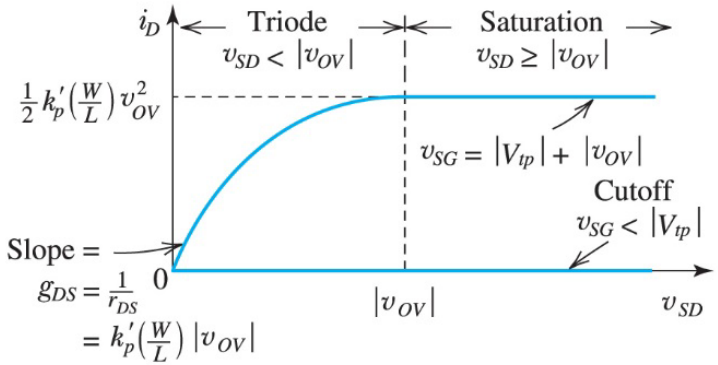


Figure 5.13 The $i_D - v_{DS}$ characteristics for an enhancement-type NMOS transistor

- P-channel MOSFET symbols and characteristics

Table 5.2 Regions of Operation of the Enhancement PMOS Transistor





- $v_{SG} < |V_{tp}|$: no channel; transistor in cutoff; $i_D = 0$
- $v_{SG} = |V_{tp}| + |v_{OV}|$: a channel is induced; transistor operates in the triode region or in the saturation region depending on whether the channel is continuous or pinched off at the drain end;

Triode Region

Continuous channel, obtained by:

$$v_{DG} > |V_{tp}|$$

or equivalently

$$v_{SD} < |v_{OV}|$$

Then

$$i_D = k_p'\left(\frac{W}{L}\right)\left[(v_{SG} - |V_{tp}|)v_{SD} - \frac{1}{2}v_{SD}^2\right]$$

or equivalently

$$i_D = k_p'\left(\frac{W}{L}\right)\left(|v_{OV}| - \frac{1}{2}v_{SD}\right)v_{SD}$$

Saturation Region

Pinched-off channel, obtained by:

$$v_{DG} \leq |V_{tp}|$$

or equivalently

$$v_{SD} \geq |v_{OV}|$$

Then

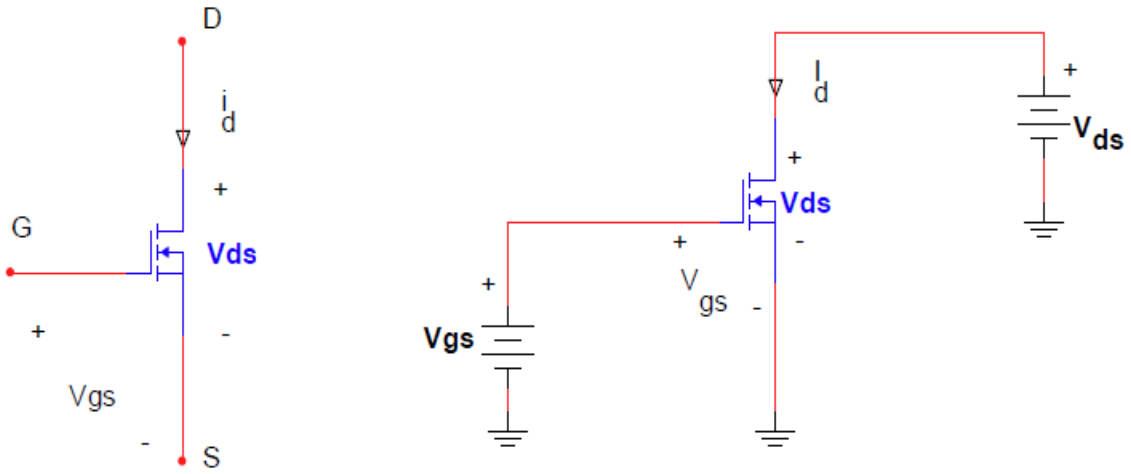
$$i_D = \frac{1}{2}k_p'\left(\frac{W}{L}\right)(v_{SG} - |V_{tp}|)^2$$

or equivalently

$$i_D = \frac{1}{2}k_p'\left(\frac{W}{L}\right)v_{OV}^2$$

- Experiment 7

Set up the following circuit with an enhancement nMOSFET (**2N7000**).



Do a quick measurement for all cases below.

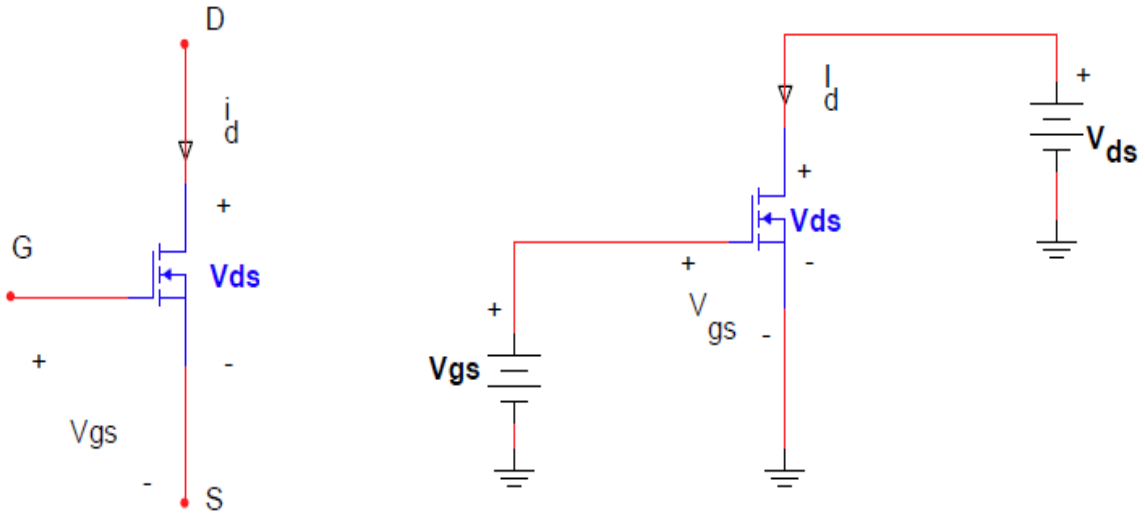
a) Select $V_{GS} = 2.8V$

b) Measure I_D as a function of V_{DS} and graph $\boldsymbol{I_D - V_{DS}}$**. Obtain at least five points in the triode region and three points in the saturation region.**

V_{DS} (V)	0	0.1	0.2	0.3	0.4	0.5	0.6	0.7	0.8	0.9	1.0	1.1	1.2
I_D $(V_{GS} = 2.8V)$													
I_D $(V_{GS} = 3.0V)$													
I_D $(V_{GS} = 3.2V)$													

- Experiment 7

Set up the following circuit with an enhancement nMOSFET (**2N7000**).



Do a quick measurement for all cases below.

c) Identify the triode and saturation regions in the graph

d) Estimate the threshold voltage, V_t

e) Estimate k_n

Briefly explain and comment your results.

5.3 MOSFET circuit at DC

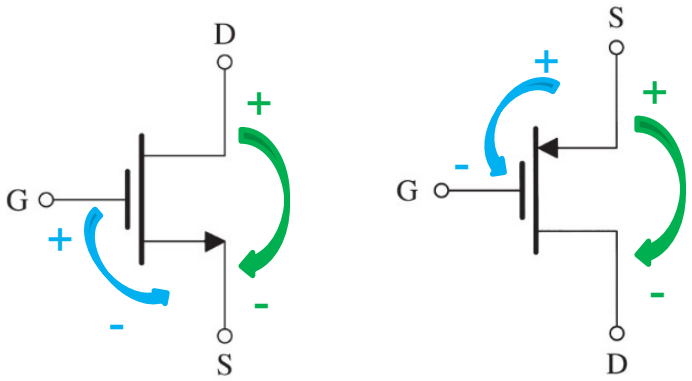
- In which mode is the transistor operating?

  Top-Bottom-Threshold rule (TBT)

  – First TBT (GS/SG VS. V_t)?
    - TB > $|V_t|$ ($V_{GS} > |V_{tn}|$ for NMOS, $V_{SG} > |V_{tp}|$ for PMOS) => Conducting
    - TB < $|V_t|$ => Cutoff

  – Second TBT (DS/SD VS. V_{OV})?
    - TB > V_{OV} ($V_{DS} \geq V_{OV}$ for NMOS, $V_{SD} \geq V_{OV}$ for PMOS) => Saturation
    - TB < V_{OV} => Triode

$V_{OV} = V_{GS} - V_{tn}$ *for NMOS*
$V_{OV} = V_{SG} - |V_{tp}|$ *for PMOS*



- Analysis procedure
  - Find conduction (GS/SG VS. V_t: 1st TBT rule)
    - If conducting -> assume in saturation mode first
    - If not conducting, in cutoff
  - Proceeds all currents and voltages
  - Find saturation (DS/SD VS. V_{OV}: 2nd TBT rule)
    - In saturation
    - If not saturated, in triode mode -> redo the analysis

Another solution to find saturation:

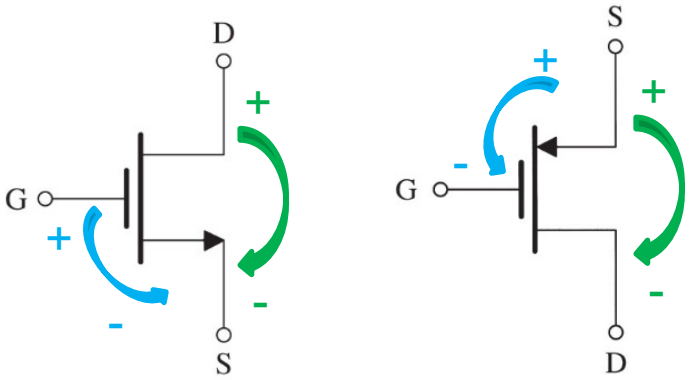
$V_{DS} > V_{OV}$ => $V_D - V_S > V_G - V_S - V_{tn})$ =>

$V_{DG} > -V_{tn}$ $(V_{DG} \geq 0)$

For PMOS,

$V_{SD} > V_{OV}$ => $V_S - V_D > V_S - V_G - |V_{tp}|)$ =>

$V_{GD} > -|V_{tp}|$ $(V_{GD} \geq 0)$



- # Example 5.3

Design the circuit: determine the values of R_D and R_S so that the transistor operates at $I_D = 0.4mA$ and $V_D = 0.5V$. The NMOS transistor has $V_t = 0.7V$, $u_n C_{ox} = 100uA/V^2$, $L = 1um$, and W$= 32um$. Neglect the channel-length modulation effect ($\lambda = 0$).

$$R_D = \frac{2.5 - V_D}{I_D} = \frac{2.5 - 0.5}{0.4} = 5k\Omega$$

Glancing $V_D > V_G$ ($V_{DS} > V_{GS}$), so the transistor in saturation.

$$k_n = u_n C_{ox}\left(\frac{W}{L}\right) = 100 \times \frac{32}{1} = 3.2\frac{mA}{V^2}$$

$$I_D = \frac{1}{2}k_n {V_{OV}}^2 \Rightarrow 0.4 = \frac{1}{2} \times 3.2 \times {V_{OV}}^2 \Rightarrow V_{OV} = 0.5V$$

$$V_{GS} - V_t = 0.5V, \text{ thus } V_G - V_S - V_t = 0.5V \Rightarrow V_S = -1.2V$$

$$R_S = \frac{-1.2V - (-2.5V)}{I_D} = 3.25k\Omega$$

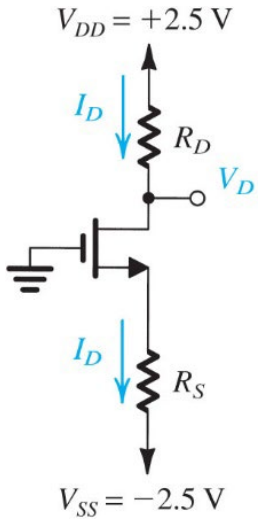


Figure 5.21 Circuit for Example 5.3.

- Example 5.4 (diode-connected transistor)

Find the $i - v$ relationship in terms of the MOSFET parameters $k_n = k_n'\left(\frac{W}{L}\right)$ and V_{tn}. Neglect the channel-length modulation ($\lambda = 0$).

Note that this two-terminal device is known as a diode-connected transistor.

Since $V_D = V_G$ implies operation in the saturation region.

$$I_D = \frac{1}{2}k_n'\left(\frac{W}{L}\right)(V_{GS} - V_{tn})^2$$

So $I_D = \frac{1}{2}k_n(v - V_{tn})^2$

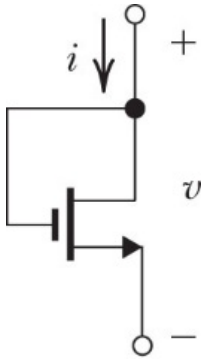


Figure 5.22

- Example 5.5

Design a circuit (Find R_D) to establish a drain voltage of $V_D = 0.1V$. What is the effective resistance between drain and source at this operating point (r_{DS})? Let $V_{tn} = 1V$, $k_n'(W/L) = 1\,mA/V^2$

Since $V_{DS}(0.1V) < V_{OV}$ $(V_{GS} - V_{tn} = 5 - 1 = 4V)$,
the transistor operates in triode region.

$$I_D = k_n'\left(\frac{W}{L}\right)\left[V_{OV} - \frac{1}{2}V_{DS}\right]V_{DS} = 1 \times (4 - 0.05) \times 0.1 = 0.395mA$$

$$R_D = \frac{5V - 0.1V}{I_D} = 12.4k\Omega$$

$$r_{DS} = \frac{0.1V}{I_D} = 253\Omega$$

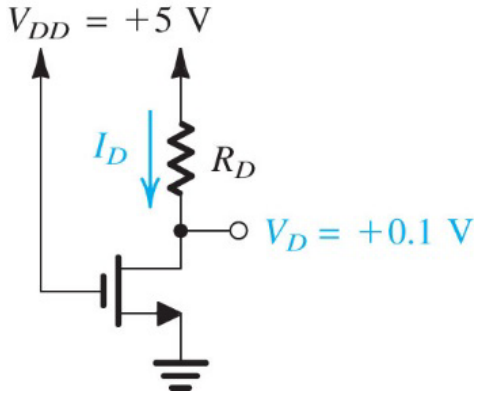
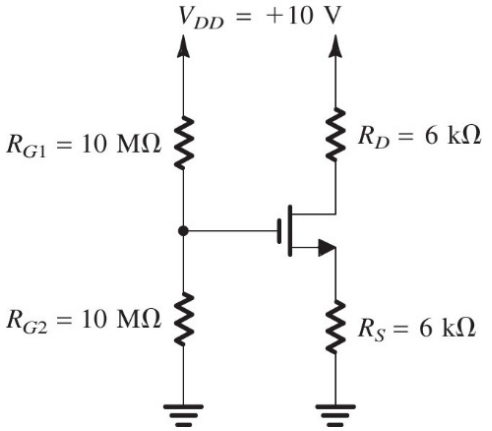


Figure 5.23 Circuit for Example 5.5.

• Example 5.6

Analyze the circuit to determine the voltages at all nodes and the currents through all branches. Let $V_{tn} = 1V$, $k_n'(W/L) = 1\,mA/V^2$. Neglect the channel-length modulation effect ($\lambda = 0$).



$$V_G = \frac{1}{2}V_{DD} = 5V$$

Since $V_G = 5V$ and V_s is grounded through a $6k\Omega$ resistor, the transistor is turned on. Assume that the transistor operates in saturation region.

$$V_S = I_D \times 6k\Omega$$

$$I_D = \frac{1}{2}k_n'(W/L)\,(V_{GS} - V_{tn})^2 = \frac{1}{2} \times 1 \times (5 - 6I_D - 1)^2$$

$$\Rightarrow\ 18I_D^2 - 25I_D + 8 = 0$$

This equation yields two values for I_D: 0.5mA and 0.89mA

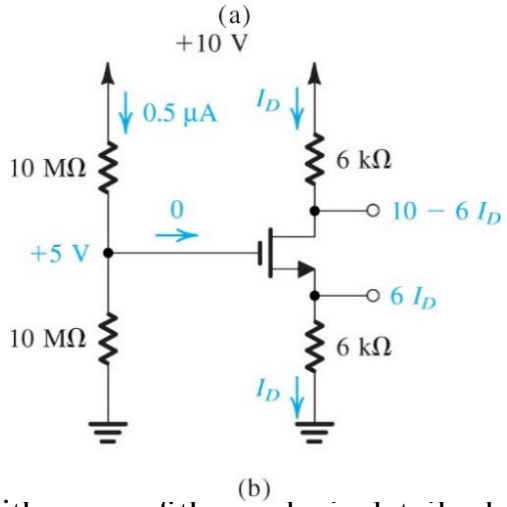


Figure 5.24 (a) Circuit for Example 5.6. **(b)** The circuit with some of the analysis details shown

• Example 5.6 Cont.

Analyze the circuit to determine the voltages at all nodes and the currents through all branches. Let $V_{tn} = 1V$, $k_n'(W/L) = 1\,mA/V^2$. Neglect the channel-length modulation effect ($\lambda = 0$).

① If $I_D = 0.89\text{mA}$, $V_S = I_D \times 6k\Omega = 5.34V > V_G$, doesn't make physical sense, should cutoff the transistor.

② Thus, $I_D = 0.5\text{mA}$

$V_S = I_D \times 6 = 3V$, $V_D = 10 - I_D \times 6 = 7V$

Since $V_{GS} = 5V - 3V = 2V$, $V_{DS} = 7V - 3V = 4V$

$V_{DS} > V_{GS} - V_{tn}$, in saturation region.

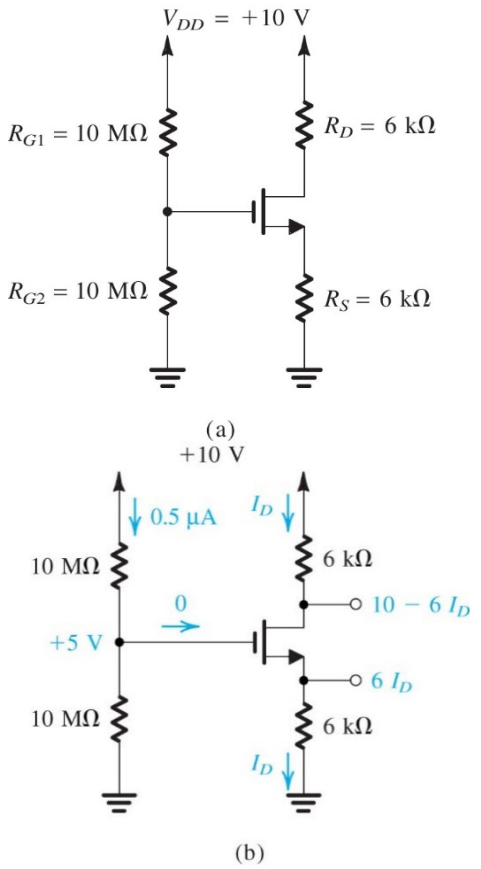


Figure 5.24 (a) Circuit for Example 5.6. **(b)** The circuit with some of the analysis details shown.

• Example 5.7

a) Find R_{G1}, R_{G2}, and R_D so that the transistor operates in saturation with $I_D = 0.5mA$, $V_D = 3V$. Let the PMOS have $V_{tp} = -1V$, $k'_p(W/L) = 1\,mA/V^2$.

b) What is the largest value that R_D can have while the transistor remains in the saturation mode? Neglect the channel-length modulation effect ($\lambda = 0$).

(a) $I_D = \frac{1}{2}k'_p\left(\frac{W}{L}\right){V_{OV}}^2 \Rightarrow V_{OV} = 1V \Rightarrow V_{SG} = V_{OV} + |V_{tp}| = 2V$

Thus $V_S - V_G = 2V \Rightarrow V_G = 5V - 2V = 3V$

This can be achieved by appropriate selection of

$R_{G1} = 2M\Omega$, $R_{G2} = 3M\Omega$

$$R_D = \frac{V_D}{I_D} = \frac{3}{0.5} = 6k\Omega$$

(b) At the edge, $V_{SD} = V_S - V_D = |V_{OV}| = 1V$

$V_{Dmax} = V_S - |V_{OV}| = 4V$ thus $R_{Dmax} = \frac{V_{Dmax}}{I_D} = 8k\Omega$

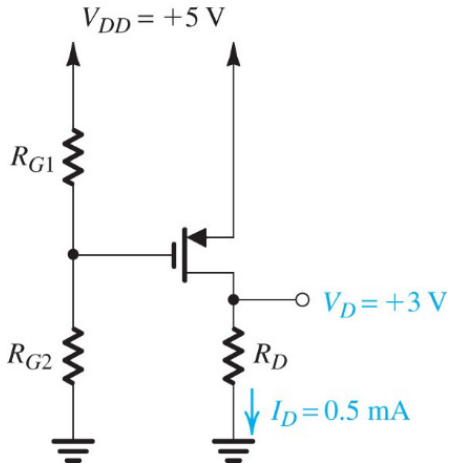


Figure 5.25 Circuit for Example 5.7.

HW5

- Problems
  - PP.294, 5.18 – Current-Voltage Characteristics #1
  - PP.297, 5.38 – Current-Voltage Characteristics #2
  - PP.299, 5.44 – MOSFET Circuit at DC #1
  - PP.299, 5.49 – MOSFET Circuit at DC #2
  - PP.300, 5.54 – MOSFET Circuit at DC #3
- Submission requirement:
  - Add the cover page!!!
  - Print the HW5.pdf out and answer all the questions
- HW5 Due: TBA (Late assignments: 40% deduction.)