CHAPTER 4

Diodes

Outline

- 4.1 The ideal diode
- 4.2 Terminal characteristics of junction diodes
- 4.3 Modeling the diode forward characteristics
- 4.5 Rectifier circuits
- 4.6 Limiting and clamping circuits

4.1 The ideal diode

- 4.1.1 Current-voltage characteristic (non-linear/piecewise linear)
  - Reverse bias: open circuit/cut off, $v < 0, i = 0$
  - Forward bias: short circuit/turn on, $v = 0, i > 0$

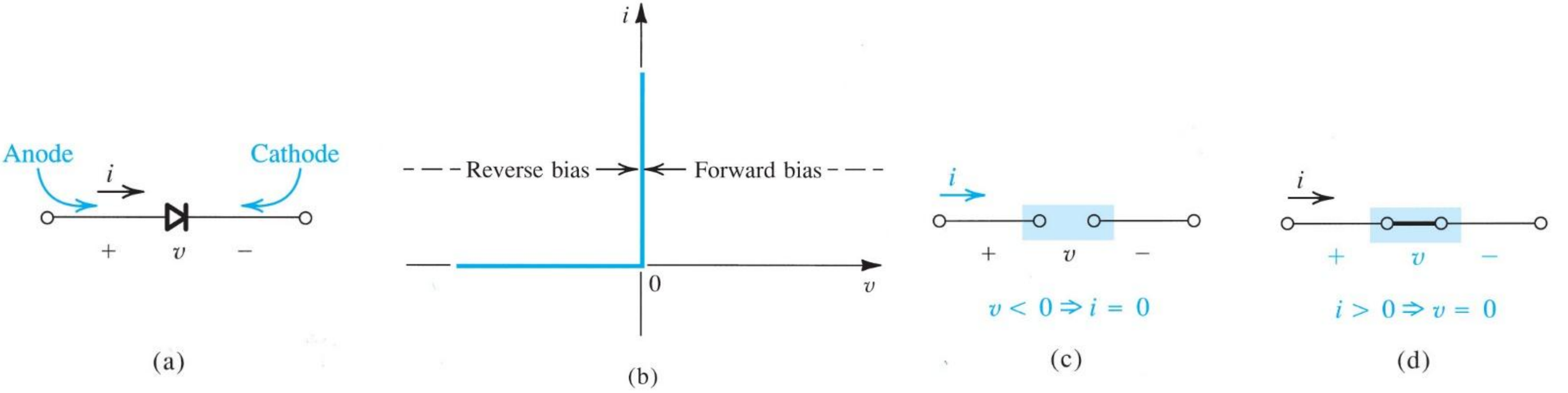


Figure 4.1 The ideal diode: **(a)** diode circuit symbol; **(b)** *i*–*v* characteristic; **(c)** equivalent circuit in the reverse direction; **(d)** equivalent circuit in the forward direction.

- Voltage dropped across the diode (v) and the current flows through the diode (i)
  - Fig. 4.2(a): conducting diode/short circuit, $v = 0, i = \frac{v}{R} = \frac{10V}{1k\Omega} = 10mA$
  - Fig. 4.2(b): cut off/open circuit, $v = 10V, i = 0mA$

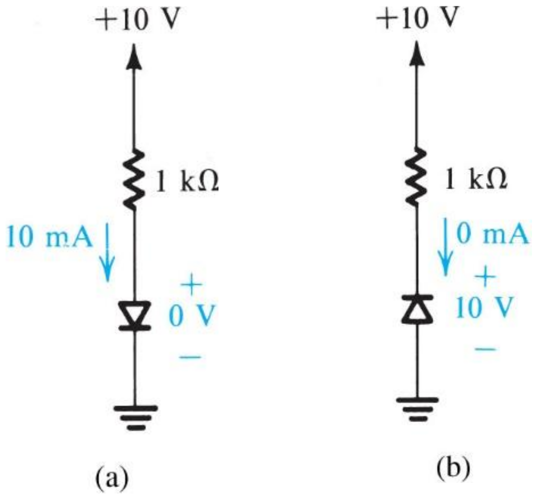


Figure 4.2 The two modes of operation of ideal diodes and the use of an external circuit to limit **(a)** the forward current and **(b)** the reverse voltage.

- 4.1.2 A simple application: the rectifier
  - Can be used to generate dc from ac

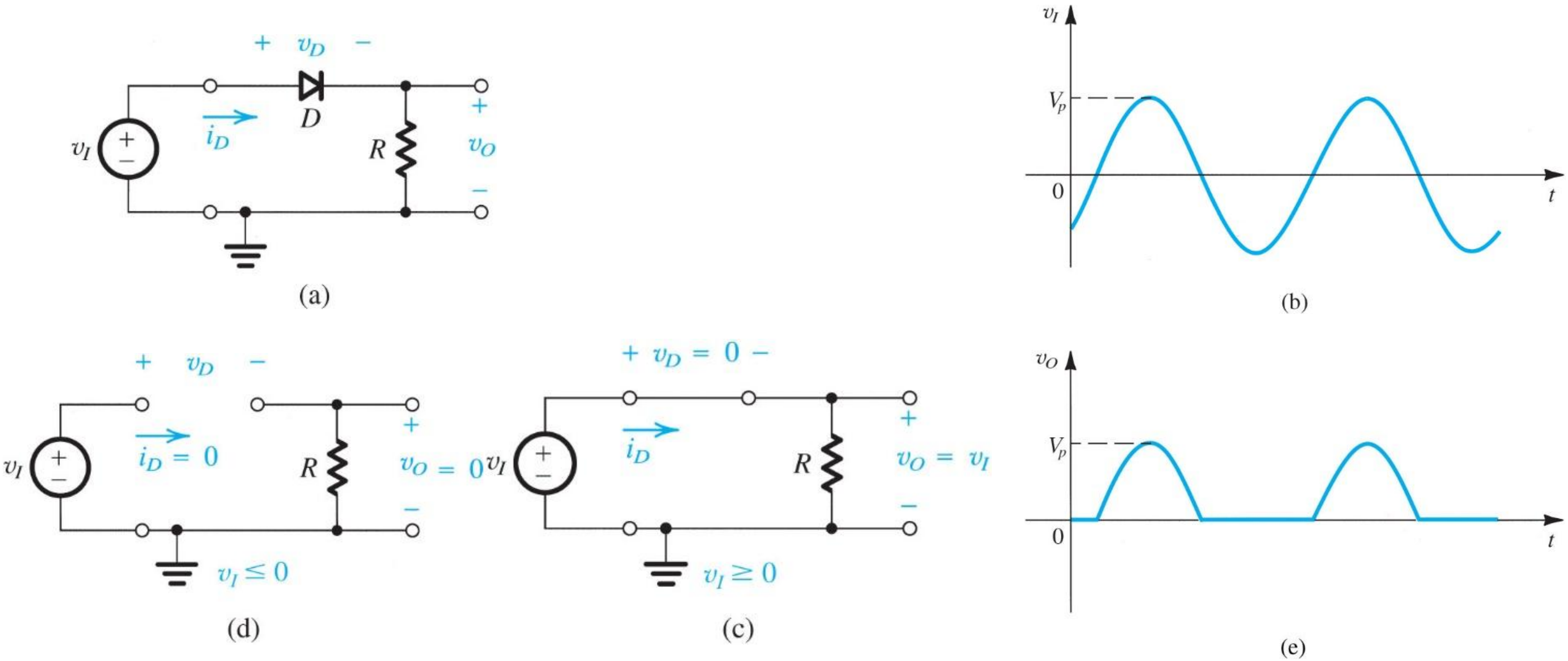


Figure 4.3 **(a)** Rectifier circuit. **(b)** Input waveform **(c)** Equivalent circuit when $v_I \geq 0$. **(d)** Equivalent circuit when $v_I \leq 0$. **(e)** Output waveform

4.2 Terminal characteristics of junction diodes

The characteristic curve consists of 3 distinct regions.

- Forward-bias: $v > 0$;
- Reverse-bias: $v < 0$;
- The breakdown region: v $< -V_{ZK}$;

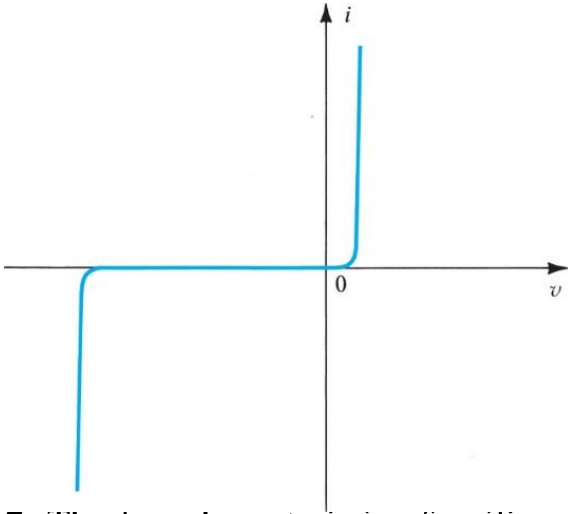


Figure 4.7 The i–v characteristic of a silicon junction diode.

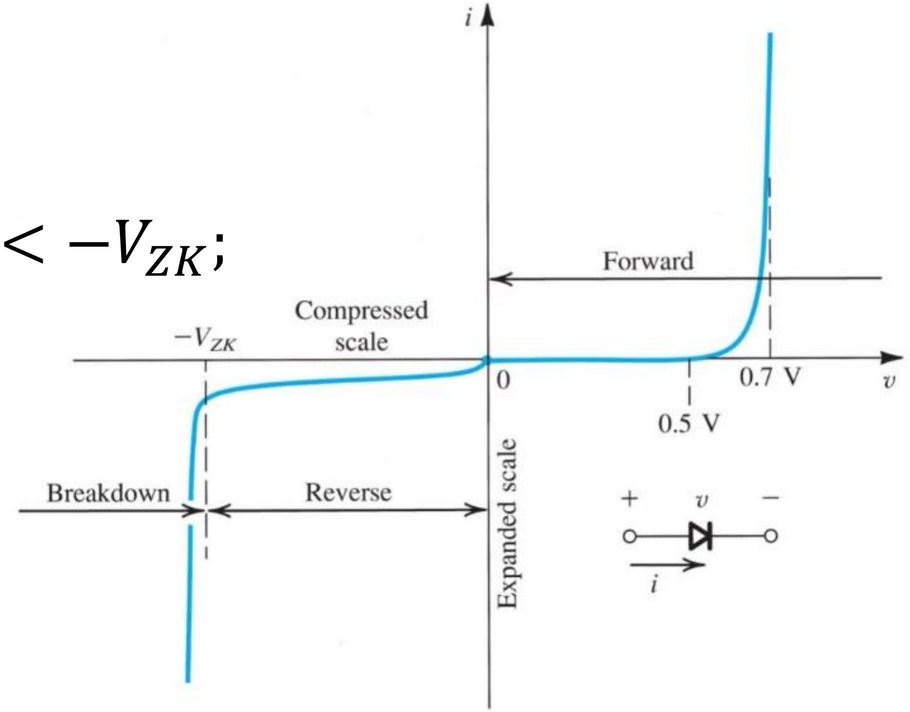


Figure 4.8 The diode i-v relationship with some scales expanded and others compressed in order to reveal details.

- 4.2.1 The forward-bias region

  $i = I_s e^{v/v_T}$

  - I_s: saturation current/scale current, very strong function of temperature
  - v_T: thermal voltage, $\approx 25mV$ at room temperature

or $v = v_T \ln \frac{i}{I_s}$, where ln is the natural logarithm.

- Example 4.3

A silicon diode said to be 1-mA device displays a forward voltage of 0.7-V at a current of 1mA. Evaluate the junction scaling constant I_s.

What scaling constants I_s would apply for a 1-A diode of the same manufacture that conducts 1-A at 0.7-V.

(a) $i = I_s e^{v/v_T}$, so $I_s = ie^{-v/v_T}$,

$$I_s = 1mA \times e^{-0.7V/25mV} = 6.9 \times 10^{-16} A$$

(b) $I_s = 1A \times e^{-0.7V/25mV} = 6.9 \times 10^{-13} A$

- # The forward-bias region

$\ln x \sim lgx$ => $y = lgx$ => $x = 10^y$
=> $\ln x = y \times ln10 = 2.3y = 2.3lgx$

If $I_1 = I_s e^{v_1/v_T}$, $I_2 = I_s e^{v_2/v_T}$,

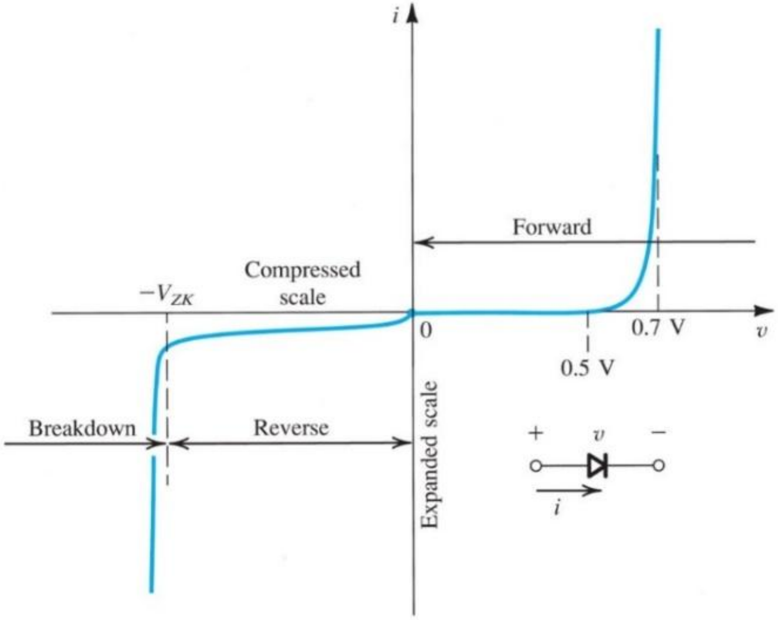
$\frac{I_1}{I_2} = e^{(v_1-v_2)/v_T}$ or $v_1 - v_2 = v_T \ln\frac{I_1}{I_2}$ or

$v_1 - v_2 = 2.3 v_T \lg\frac{I_1}{I_2}$, lg is base-10 logarithms

- **Conclusion #1**: for a decade current change, the diode voltage changes by $2.3v_T$, which is approximately 60 mV. So

  $$v_1 - v_2 = 0.06 \times \lg\frac{I_1}{I_2}$$

- **Conclusion #2**:
  - < 0.5V (**cut-in**), the current is negligibly small
  - 0.6~0.8V, rapid increase of I
  - A simple model for the diode – a conducting diode has approximate a **0.7-V drop across** it.



- # Exercise 4.6

Find the change in diode voltage if the current changes from 0.1mA to 10mA.

$$v_1 - v_2 = 2.3 v_T \lg\frac{I_1}{I_2} = 2.3 \times 25mV \times \lg\frac{10mA}{0.1mA} = 115mV$$

Or approximately, $\approx 2 \times 60mV = 120mV$

- # Exercise 4.7

A silicon junction diode has v $= 0.7V$ at $i = 1mA$. Find the voltage drop at $i = 0.1mA$ and $i = 10mA$

$v_1 - v_2 = 0.025 \ln\frac{I_1}{I_2}$, so $v_1 = v_2 + 0.025 \ln\frac{I_1}{I_2} = 0.7V + 0.025 \times \ln\frac{I_1}{1}$

For $i = 0.1mA$, $v_1 = 0.7V + 0.025 \times \ln\frac{0.1}{1} = 0.64V$

For $i = 10mA$, $v_1 = 0.7V + 0.025 \times \ln\frac{10}{1} = 0.76V$

Or approximately, $v_1 = 0.7V + 0.06 \times \lg\frac{0.1}{1} = 0.64V$ for $i = 0.1mA$

and $v_1 = 0.7V + 0.06 \times \lg\frac{10}{1} = 0.76V$ for $i = 10mA$

- 4.2.2 The reverse-bias region

  $i \approx -I_s$, I_s saturation current

- 4.2.3 The breakdown region

  Breakdown voltage: V_{ZK}

  where the subscript Z stands for zener and K denotes knee

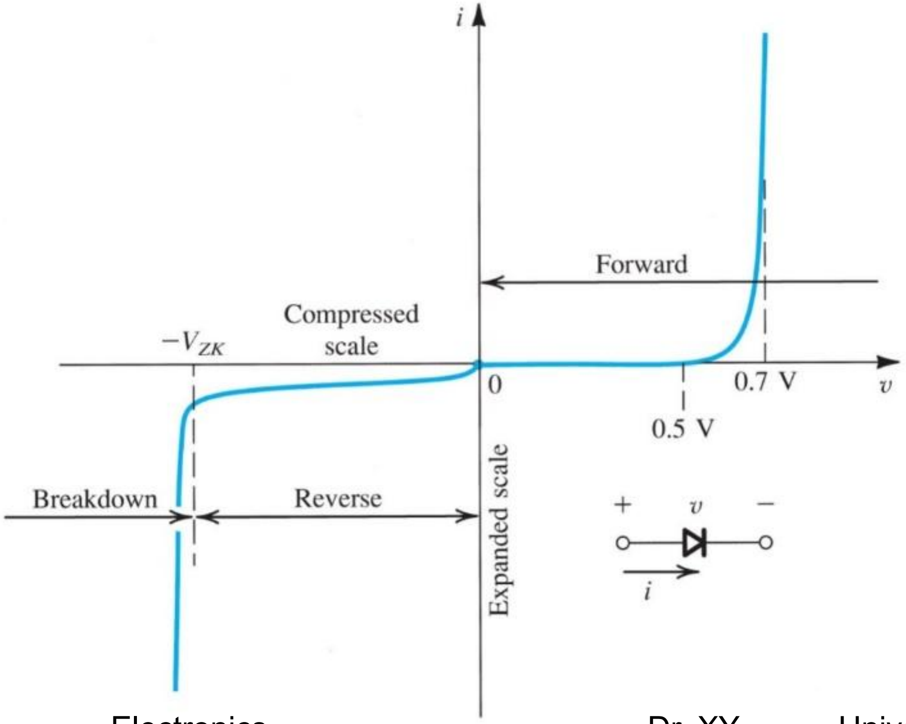


Figure 4.8 The diode i-v relationship with some scales expanded and others compressed in order to reveal details.

4.3 Modeling the diode forward characteristics

- 4.3.1 The exponential model

$$I_D = I_s e^{V_D/V_T} \quad -①$$

$$I_D = \frac{V_{DD} - V_D}{R} \quad -②$$

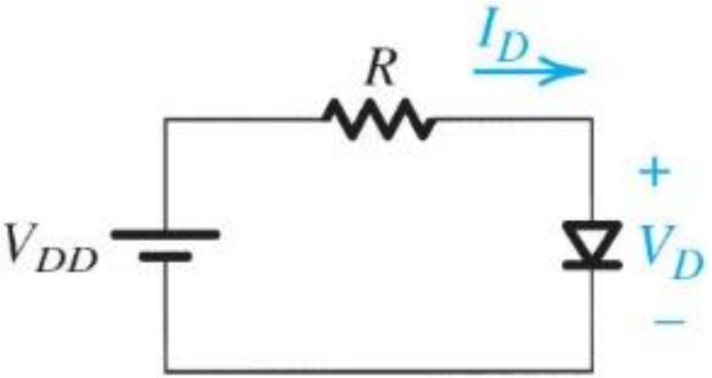


Figure 4.10 A simple circuit used to illustrate the analysis of circuits in which the diode is forward conducting.

- Exercise 4.11

Design the circuit in Fig. 4.11 to provide an output voltage of 2.4V. Assume that the diodes available have 0.7-V drop at 1mA.

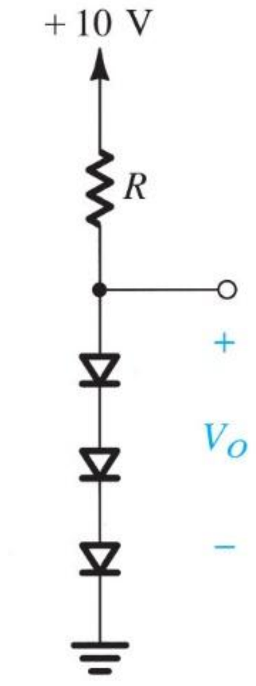


Figure E4.11

$I = I_s e^{v/v_T}$, so $I_s = I e^{-v/v_T}$,

$I_s = 1mA \times e^{-0.7V/25mV}$

When $v = \frac{2.4V}{3} = 0.8V$

$I = 1mA \times e^{-0.7V/25mV} e^{0.8V/25mV} = 54.6mA$

$R = \frac{10V - 2.4V}{54.6mA} = 139\Omega$

Alternative way:

$0.8 - 0.7 = 0.025 \times \ln \frac{I_1}{1mA}, so\ I_1 = 54.6mA$

Or $0.8 - 0.7 = 0.06 \times \lg \frac{I_1}{1mA}, so\ I_1 = 46.4mA$

4.3.3 Iterative analysis using the exponential model -- Example 4.4

Determine the current I_D and the diode voltage V_D with $V_{DD} = 5V$ and R= $1k\Omega$. Assume that the diode has a current of 1mA at a voltage of 0.7V.

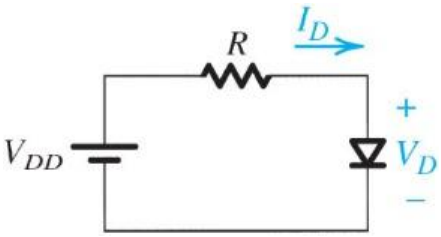
The First iteration: Assume that $V_D = 0.7V$, $I_D = \frac{V_{DD}-V_D}{R} = \frac{5V-0.7V}{1k\Omega} = 4.3mA$

Then use the conclusion #1 to obtain a better estimate for V_D

(V_2=0.7V and $I_2 = 1mA$, $I_1 = 4.3mA$)

$$V_1 = V_2 + 0.06 \times \lg\frac{I_1}{1} = 0.7V + 0.06 \times \lg\frac{4.3}{1} = 0.738V$$

Thus the first iteration are $I_D = 4.3mA$ and $V_D = 0.738V$



The second iteration: Assume that $V_D = 0.738V$, $I_D = \frac{5V-0.738V}{1k\Omega} = 4.262mA$

(V_2=0.738 V and $I_2 = 4.3mA$ and $I_1 = 4.262\ mA$)

Thus $V_1 = 0.738V + 0.06 \times \lg\frac{4.262}{4.3} = 0.738V$

Thus the second iteration are $I_D = 4.262mA$ and $V_D = 0.738V$

Since these values are very close to the values obtained after the first iteration, no further iterations are necessary.

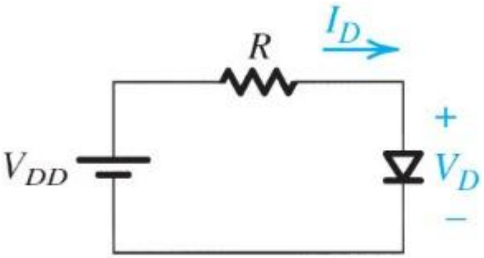
- 4.3.5 Rapid analysis using constant-voltage-drop model

$V_D = 0.7V$ (a forward-conducting diode has a voltage drop that varies in a relatively narrow range, 0.6~0.8V)

Go back to Example 4.4:

$V_{DD} = 5V$ and R= $1k\Omega$.

$$I_D = \frac{5V - 0.7V}{1k\Omega} = 4.3mA$$



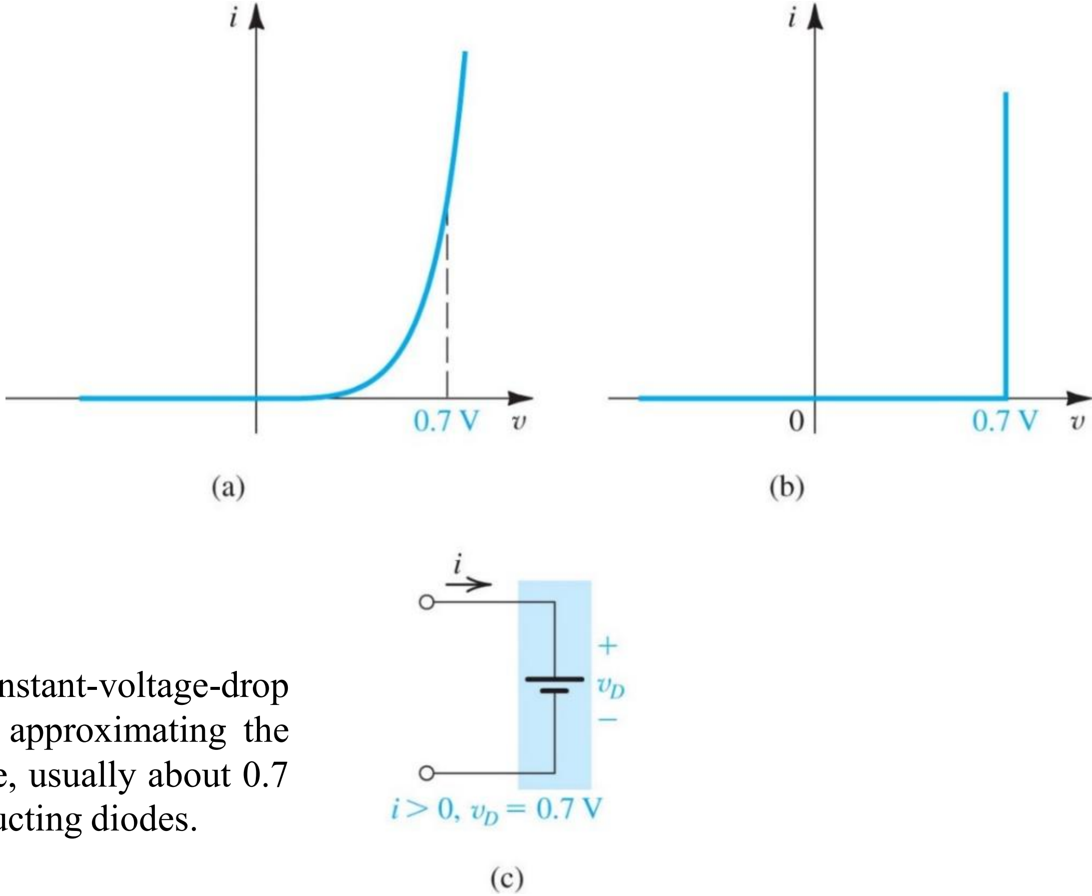


Figure 4.12 Development of the diode constant-voltage-drop model: **(a)** the exponential characteristic; **(b)** approximating the exponential characteristic by a constant voltage, usually about 0.7 V$_i$; **(c)** the resulting model of the forward-conducting diodes.

- Conclusion:
  - A diode circuit involves both dc and signal quantities.
- Equivalent Models:
  - Exponential model

$$i = I_s e^{v/v_T}$$

$$v_1 - v_2 = 0.06 \times \lg \frac{I_1}{I_2}$$

  - Constant-voltage-drop model ($V_D = 0.7V$)

4.5 Rectifier circuits

- AC power supply: 120V(rms) 60-Hz
- Transformer:
  - Primary winding (N_1 turns) and Secondary winding (N_2 turns)
  - $v_S: 120 \times \frac{N_2}{N_1}\ V(rms)$ e.g.8-V (rms) v_S, 15:1 turns ratio
- Diode rectifier: sine-wave -> unipolar output
- Filter: reduce the variations of the rectifier output
- Voltage regulator: reduce ripple (zener shunt regulator)

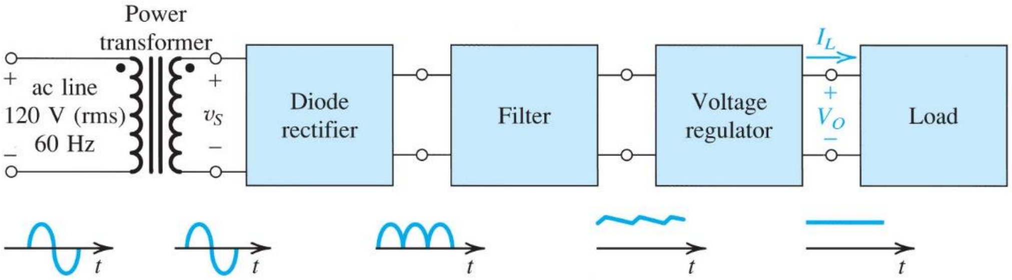


Figure 4.22 Block diagram of a dc power supply.

• 4.5.1 The half-wave rectifier

$$v_o = 0, v_S < V_D$$

$$v_o = v_S - V_D, v_S \geq V_D \qquad V_D \text{ is around 0.7V}$$

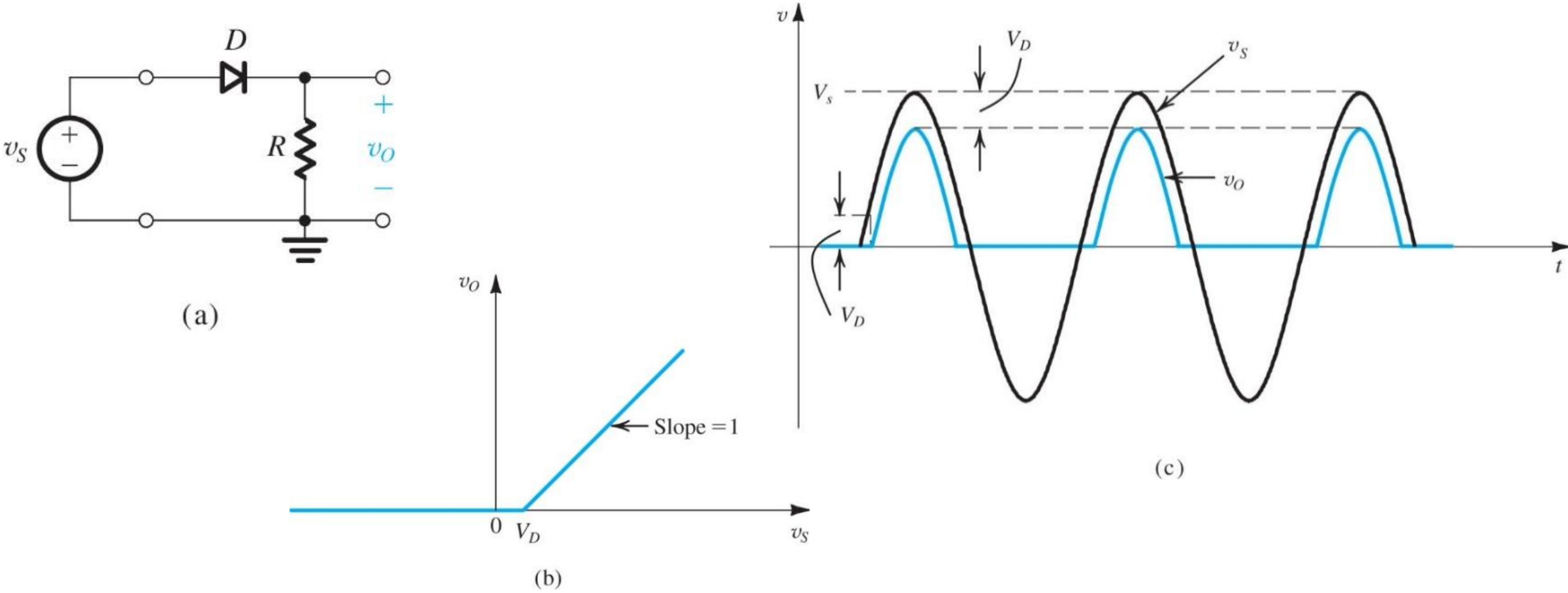


Figure 4.23 (a) Half-wave rectifier. **(b)** Transfer characteristic of the rectifier circuit. **(c)** Input and output waveforms.

- 4.5.2 The full-wave rectifier
  - **Center-tap** the transformer secondary winding
  - v_S positive half: D1 conducts, D2 reverse bias

    the circuit behaves like a half-wave rectifier
  - v_S negative half: D1 cut off, D2 conducts

    the circuit behaves again like a half-wave rectifier

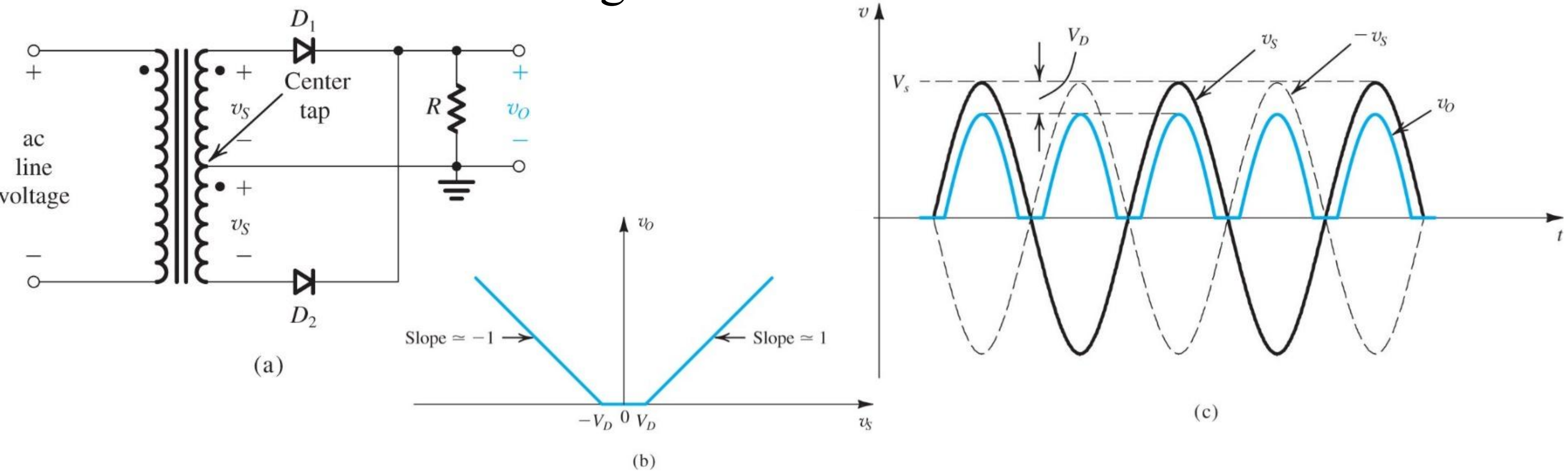
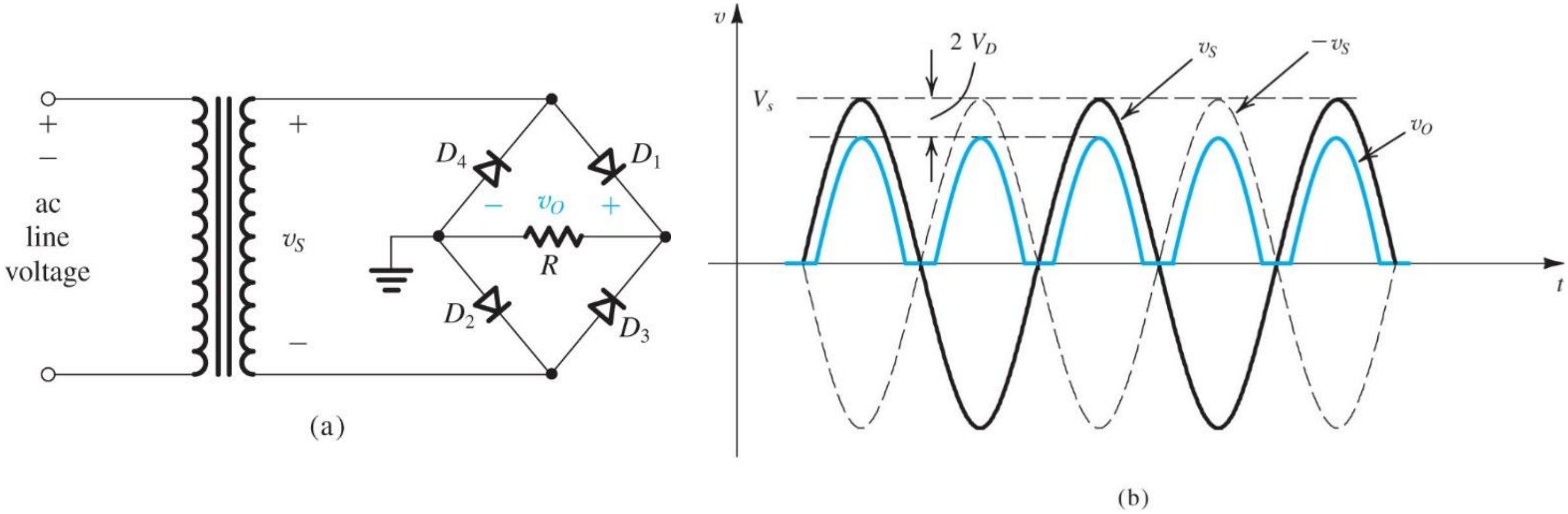


Figure 4.24 Full-wave rectifier utilizing a transformer with a center-tapped secondary winding: **(a)** circuit; **(b)** transfer characteristic assuming a constant-voltage-drop model for the diodes; **(c)** input and output waveforms.

- 4.5.3 The bridge rectifier
  - v_S positive: D1 and D2 conduct, D3 and D4 cutoff
  - v_S negative : D1 and D2 cut off, D3 and D4 conduct
  - Advantages: Don’t require a center-tap transformer
  - Disadvantages: 1) four diodes 2) double voltage drop on output



(a)

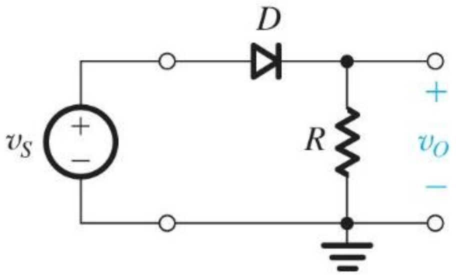
(b)

Figure 4.25 The bridge rectifier: **(a)** circuit; **(b)** input and output waveforms.

- Experimental 5.1

Do the computer simulation and set up the following circuits.

Set up the following circuit with diode (1N4148).



$v_{in}(t) = V_p \sin(\omega t)$ volts, $V_p = 5V$, $f = 60Hz$. $R = 1K\Omega$.

Measure and **graph** $v_o(t)$. Briefly explain and comment your results.

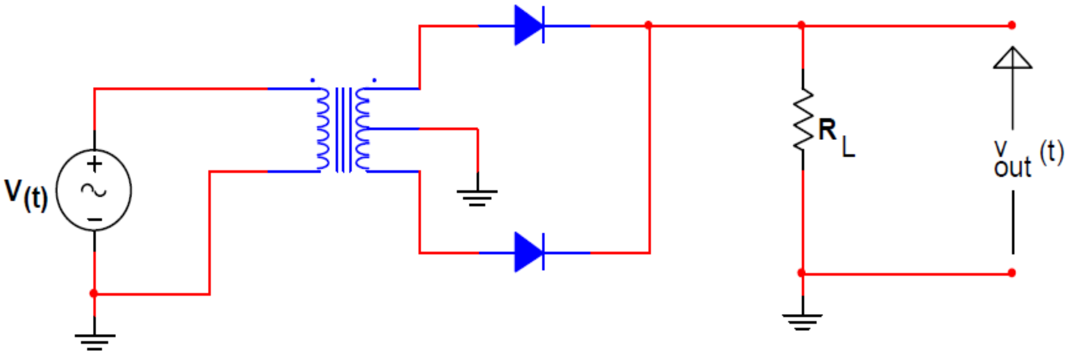
Experimental results:

$v_{in}(t)$	R	v_{omax}	v_{omin}
$V_p = 5V, f = 60Hz$	$1K\Omega$		

- Experimental 5.2

Do the computer simulation of the following circuits.

Set up the following circuit with the transformer and diode (1N4148).



Repeat the procedure 1.

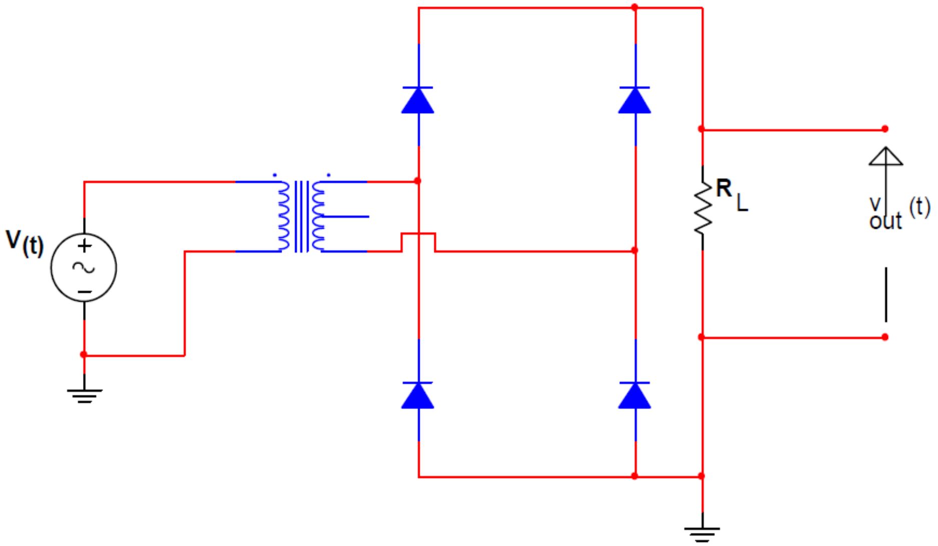
Measure and graph $v_o(t)$. Briefly explain and comment your results.

$v_{in}(t)$	R_L	v_{omax}	v_{omin}
$V_p = 40V, f = 60Hz$	$10k\Omega$		

- Experimental 5.3

Do the computer simulation of the following circuits.

Set up the following circuit with the transformer and diode (1N4148).



$v_{in}(t)$	R_L	v_{omax}	v_{omin}
$V_p = 40V, f = 60Hz$	$10k\Omega$		

$v_{in}(t) = V_p \sin(\omega t)\ \ volts$.

Measure and **graph** $v_o(t)$. Briefly explain and comment your results.

4.6 Limiting and clamping circuits

- 4.6.1 Limiter/clipping circuit: $\frac{L_-}{K} \le v_I \le \frac{L_+}{K}$
  - Clippers: the positive and/or negative peaks are clipped off
    - Used in FM transmitters where noise peaks are limited to a particular value so that excessive peaks are removed from them.
    - Used to put off the voltage beyond the preset value without disturbing the remaining part of the input waveform.

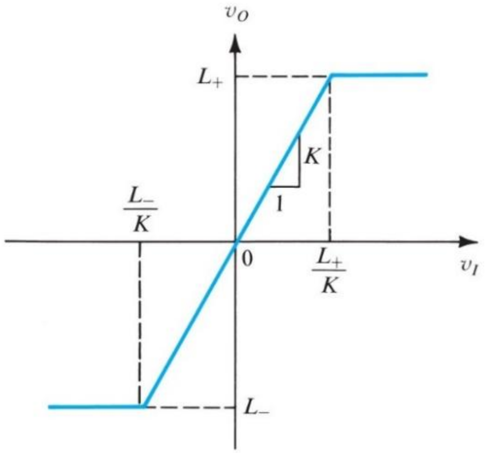


Figure 4.30 General transfer characteristic for a limiter circuit.

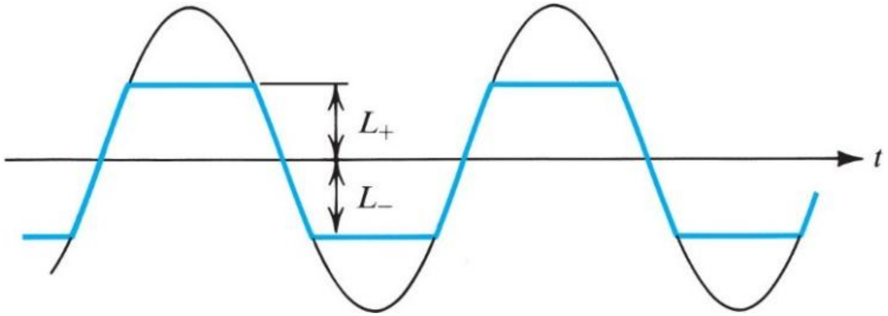
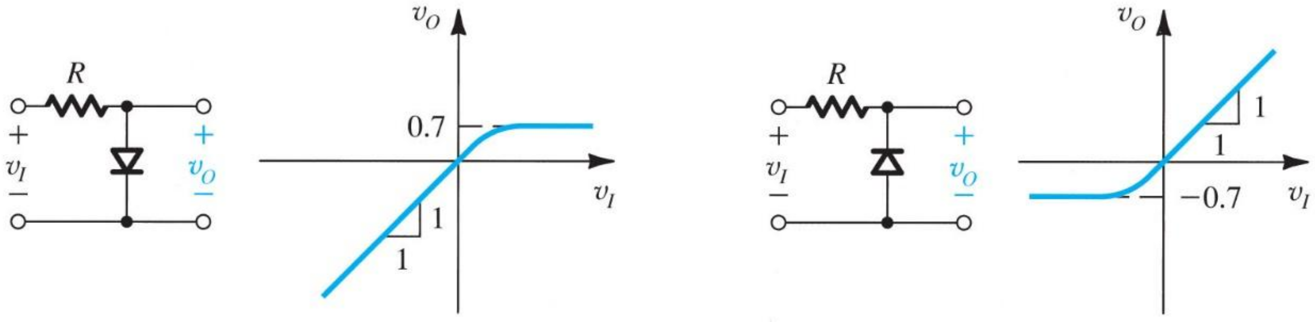


Figure 4.31 Applying a sine wave to a limiter can result in clipping off its two peaks.

- Fig. 4.33 (a)
  - $v_I < 0.5V$, diode is cut off, $v_o = v_I$
  - $v_I \geq 0.5V$, diode conducts, v_o will be saturated at one diode drop (0.7V)
- Fig. 4.33 (b)
  - $v_I > -0.5V$, diode is cut off, $v_o = v_I$
  - $v_I \leq -0.5V$, diode conducts, v_o will be saturated at one diode drop (-0.7V)



(a) (b)

Figure 4.33 A variety of basic limiting circuits. (using the constant-voltage-drop (V_D) diode model)

- Fig. 4.33 (c): double limiting
  - $-0.5V \leq v_I \leq 0.5V$, both diodes are cut off, $v_o = v_I$
  - $v_I > 0.5V$, D1 conducts, v_o will be limits to +0.7V
  - $v_I < -0.5V$, D2 conducts, v_o will be limits to -0.7V
- Fig. 4.33 (d): threshold level control
  - $v_I < 5.5V$, diode is cut off, $v_o = v_I$
  - $v_I \geq 5.5V$, diode conducts, v_o will be saturated at 5+0.7=5.7V

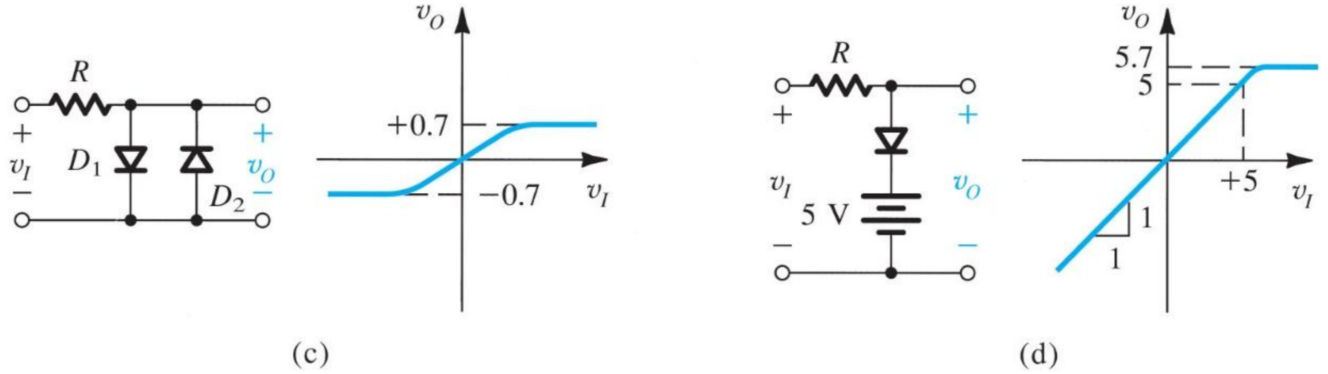


Figure 4.33 A variety of basic limiting circuits. (using the constant-voltage-drop (V_D) diode model)

- Exercise 4.26

Assume the diodes to be ideal (no 0.7V drop). Describe the transfer characteristic of the circuit.

When $-5V < v_I < 5V$, D_1 and D_2 cut off. $v_o = v_I$

When $v_I \geq 5V, D_2$ conducts, D_1 cut off

KVL: $v_I - 5 - I \times 20 = 0 \Rightarrow I = \frac{v_I - 5}{20}$

$$v_o = v_I - \mathrm{I} \times 10 = \frac{v_I}{2} + 2.5\mathrm{V}$$

When $v_I \leq -5V, D_1$ conducts, D_2 cut off

KVL: $v_I + 5 - I \times 20 = 0 \Rightarrow I = \frac{v_I + 5}{20}$

$$v_o = v_I - \mathrm{I} \times 10 = \frac{v_I}{2} - 2.5\mathrm{V}$$

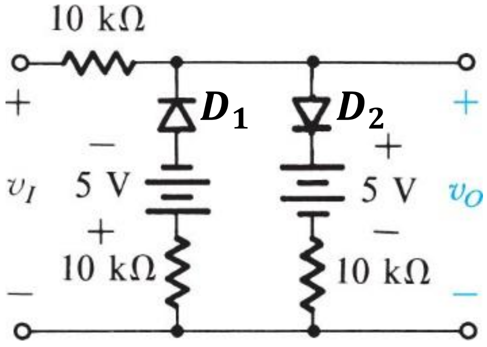


Figure E4.26

- # 4.6.2 Clamping circuit
  - Used to shift/alter either positive or negative peak of an input signal to a desired level, also called as level shifter or DC restorer. These clamping circuits can be positive or negative depends on the diode configuration.
    - Negative part: diode conducts, capacitor is charged.

      Ideal model: $v_I - v_c = 0.\ v_c = v_I = -6V$
    - Positive part: diode cut off

      Ideal model: $v_o = v_I - v_c = 4 + 6 = 10V$
    - The lowest peak clamped to 0V -> clamped circuit

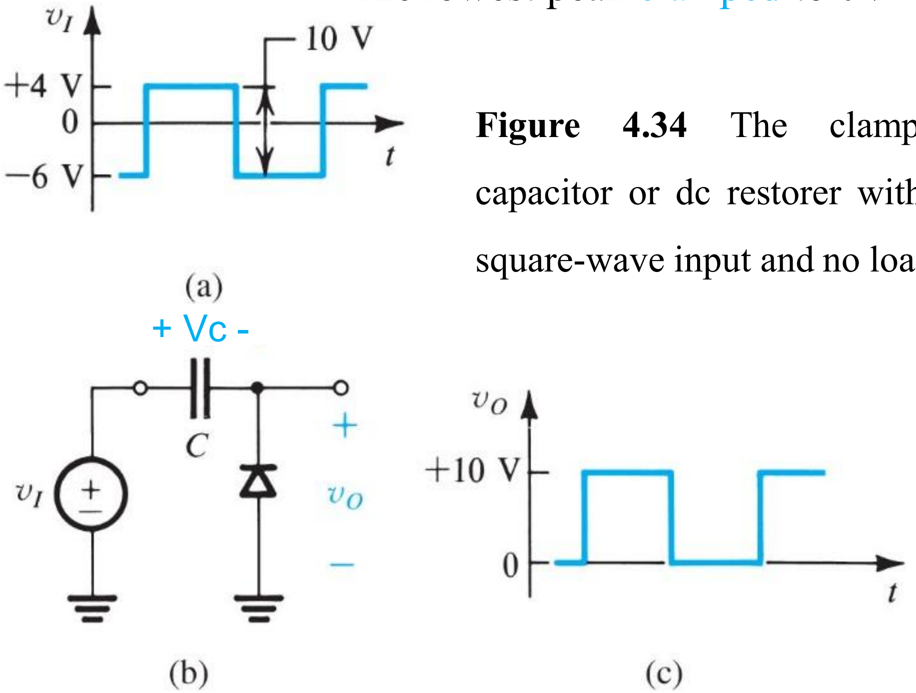
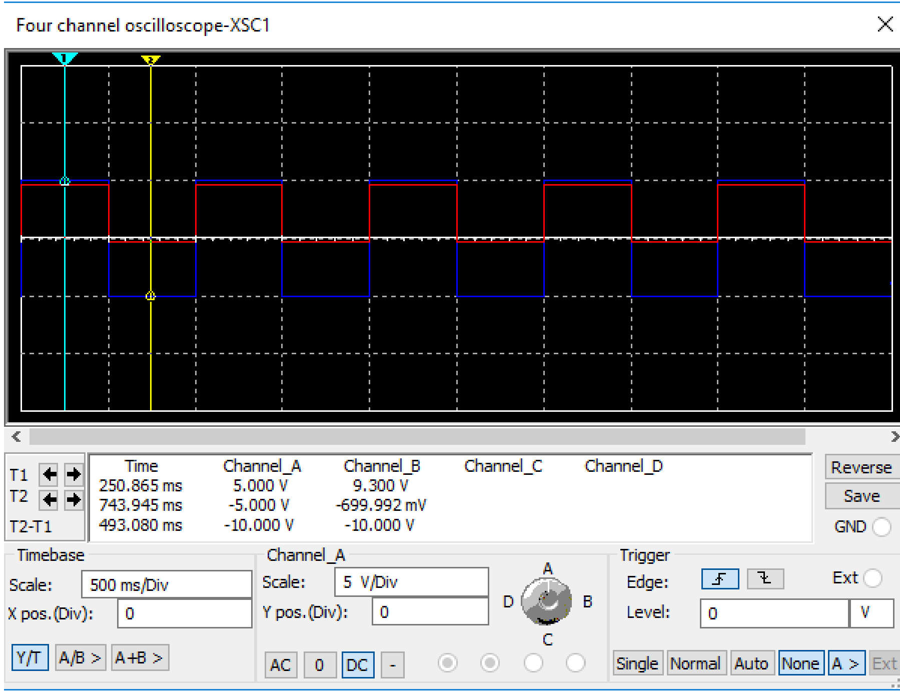


Figure 4.34 The clamped capacitor or dc restorer with a square-wave input and no load.



Time	Channel_A	Channel_B	Channel_C	Channel_D
250.865 ms	5.000 V	9.300 V		
743.945 ms	-5.000 V	-699.992 mV		
493.080 ms	-10.000 V	-10.000 V		

Timebase
Scale: 500 ms/Div
X pos.(Div): 0

Channel_A
Scale: 5 V/Div
Y pos.(Div): 0

Trigger
Edge:
Level: 0 V
Ext

- The clamped capacitor with a load resistance R
  - t_0 to t_1: discharge with time constant CR
  - t_1: v_I decreases by V_a and v_o follows; diode conducts and charge the capacitor
  - t_2: v_I rises by V_a and v_o follows
  - The charge lost by the capacitor during the interval t_0 to t_1 is recovered during the interval t_1 to t_2

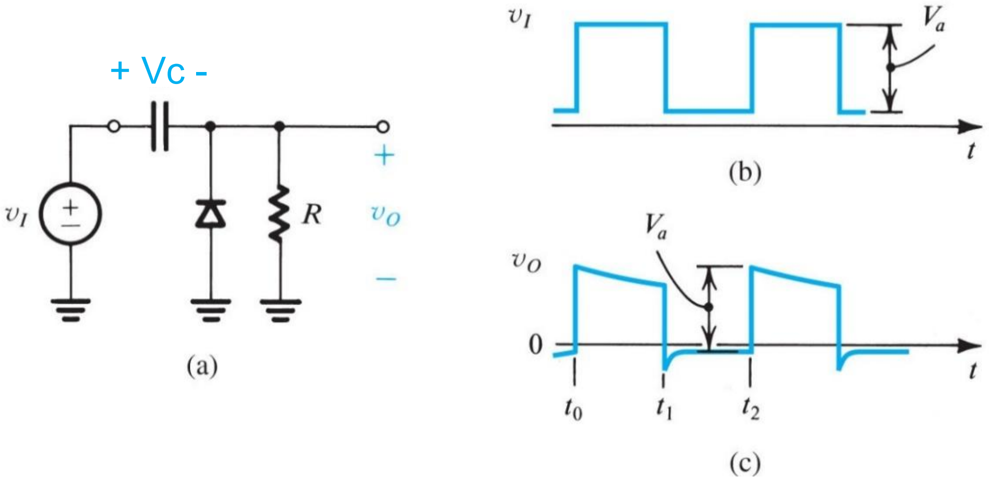
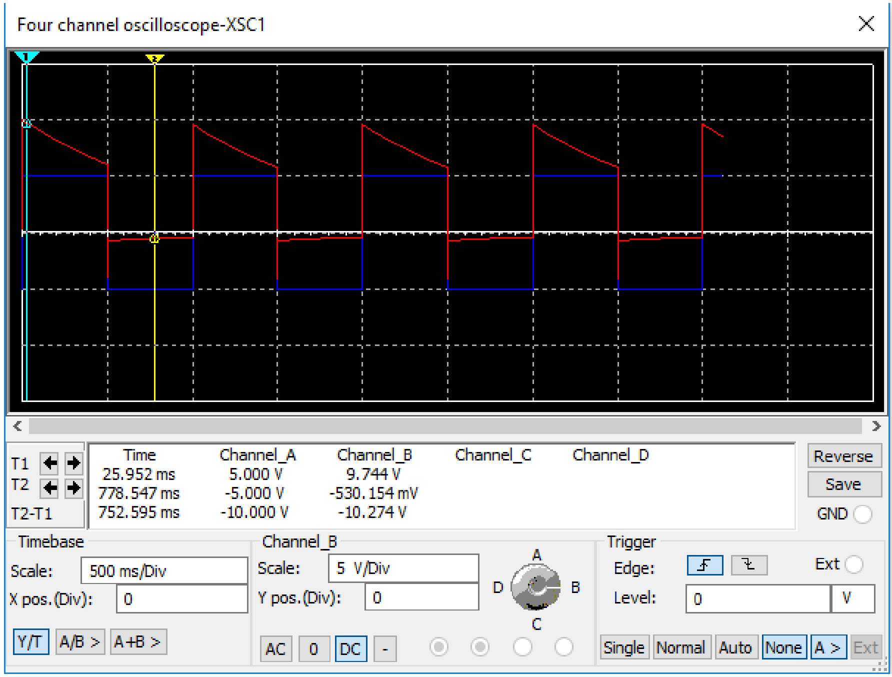


Figure 4.35 The clamped capacitor with a load resistance *R*.



	Time	Channel_A	Channel_B	Channel_C	Channel_D
T1	25.952 ms	5.000 V	9.744 V		
T2	778.547 ms	-5.000 V	-530.154 mV		
T2-T1	752.595 ms	-10.000 V	-10.274 V		

Timebase
Scale: 500 ms/Div
X pos.(Div): 0

Channel_B
Scale: 5 V/Div
Y pos.(Div): 0

Trigger
Edge:
Level: 0 V

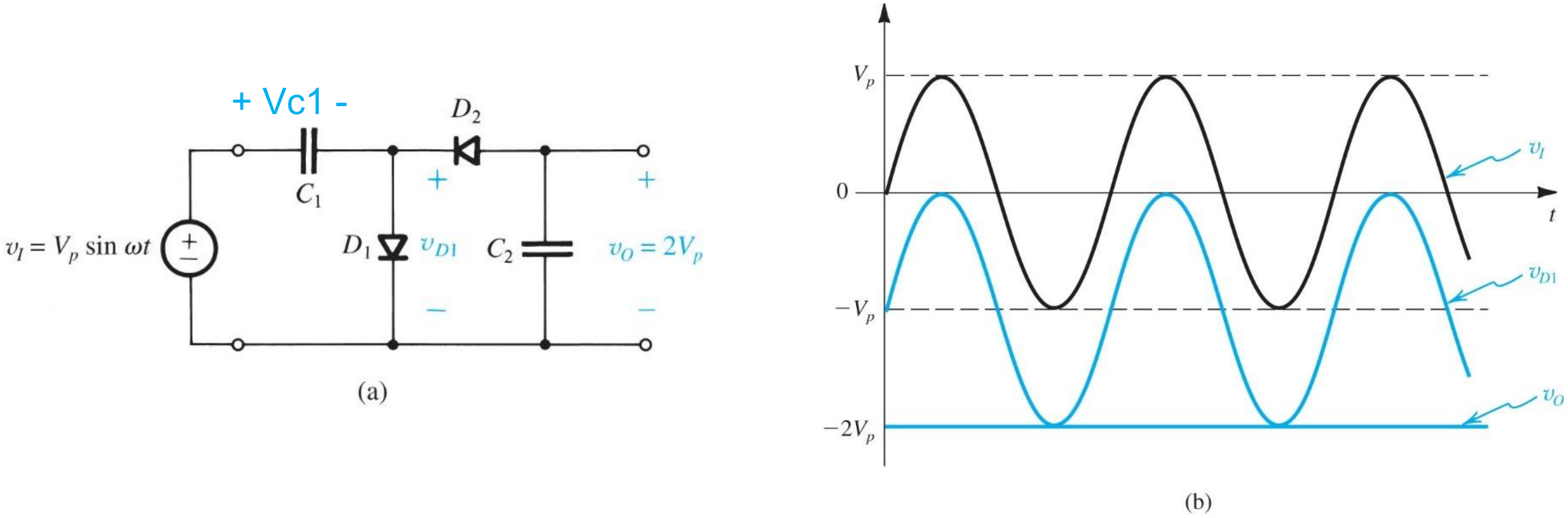
- 4.6.3 The voltage doubler
  - Positive v_I: D1 conducts, D2 cutoff

Ideal model, $v_I - v_{C1} = 0$, thus $v_{C1} = v_I|_{max} = V_P$

  - Negative v_I: D2 conducts, D1 cutoff

Ideal model, $v_{C2} + V_P - v_I = 0$,

thus $v_o = v_{C2} = v_I|_{max} - V_P = -2V_P$



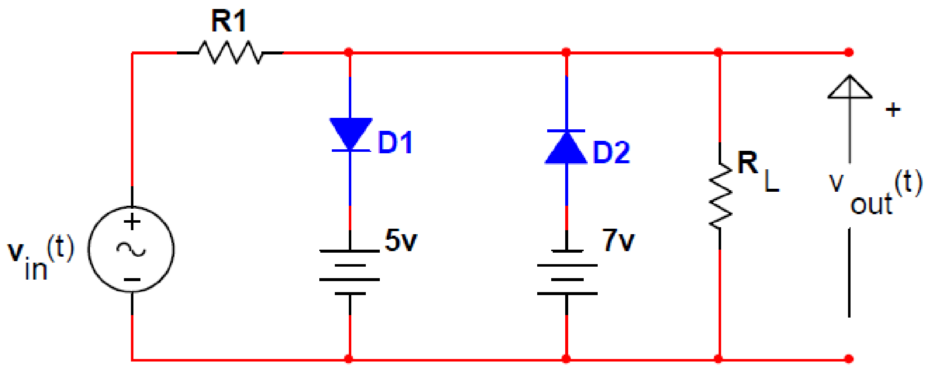
(a)

(b)

Figure 4.36 Voltage doubler: (a) circuit; (b) waveforms of the input voltage, the voltage across D1, and the output voltage $v_o = -2V_p$.

- Experiment 6.1

Set up the following circuit with diode (**1N4148**).



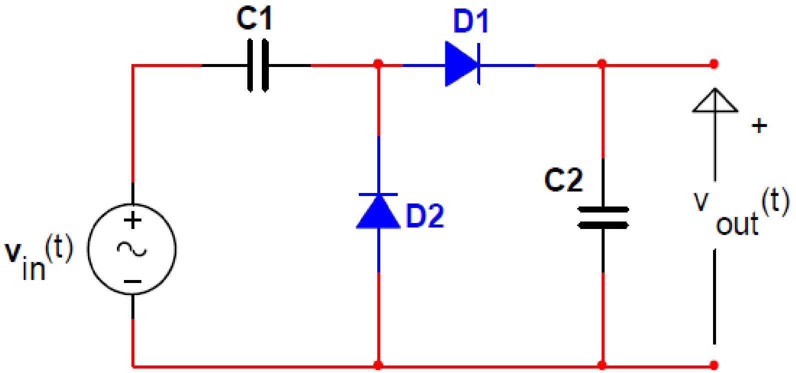
$v_{in}(t) = V_p \sin(\omega t)$ $volts$.

Measure and **graph** $v_o(t)$. Briefly explain and comment your results.

$v_{in}(t)$	R_1	R_L	v_{omax}	v_{omin}
$V_p = 10V, f = 60Hz$	100Ω	$10k\Omega$		

- Experiment 6.2

Set up the following circuit with diode (**1N4148**).



$v_{in}(t) = V_p \sin(\omega t)\ \ volts.$

Measure and **graph** $v_o(t)$. Briefly explain and comment your results.

$v_{in}(t)$	C_1	C_2	v_{omax}	v_{omin}
$V_p = 10V, f = 60Hz$	$0.1uF$	$0.1uF$		

HW3-4

- Problems
  - PP.236, 4.37 – Modeling the diode forward characteristic – the exponential model
  - PP.238, 4.56 – Modeling the diode forward characteristic – the small-signal model
  - PP.239, 4.70 – Rectifier circuits
  - PP.239, 4.96 – Limiting and Clamping Circuits
- Submission requirement:
  - Add the cover page!!!
  - Print the HW3-4.pdf out and answer all the questions (download on the blackboard)
- HW3-4 Due: TBA (Late assignments: 40% deduction)