

# CHAPTER 5

## **MOS Field-Effect Transistors (MOSFETs)**

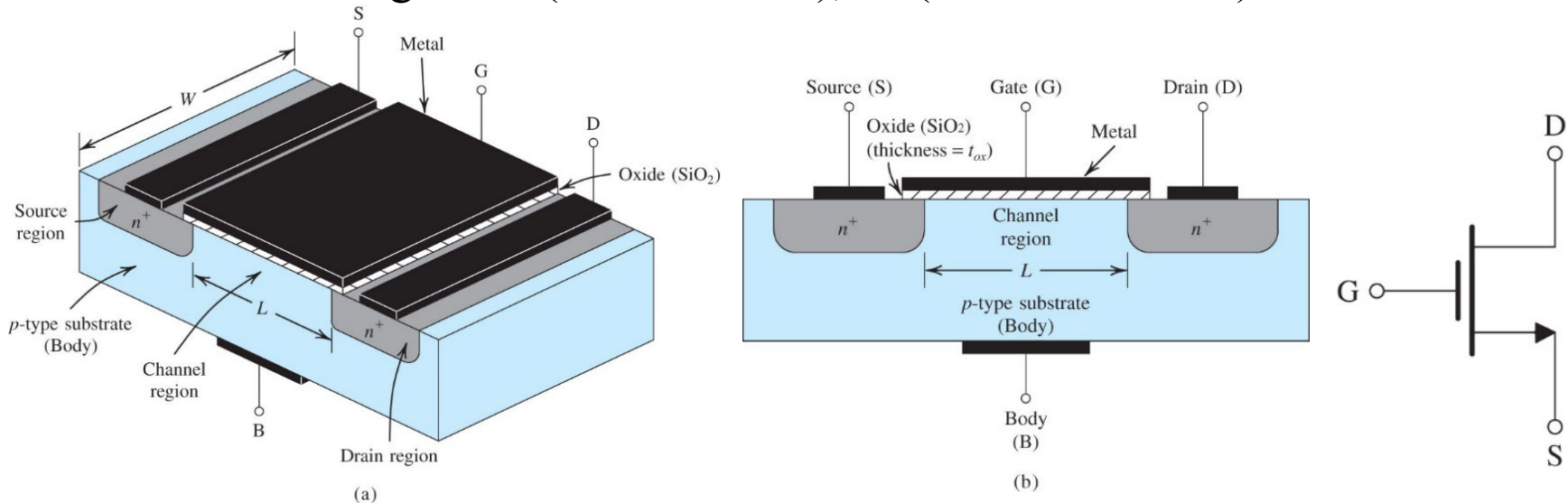
# Outline

- 5.1 Device structure and physical operation
- 14.1 CMOS Logic-Gate Circuits
- 5.2  $i_D - v_{DS}$  characteristics
- 5.3 MOSFET circuit at DC

# 5.1 Device structure and physical operation

## • 5.1.1 Device structure

- Metal-Oxide-Semiconductor FET → MOSFET **FET?**
- Three terminals: source, drain, gate, (substrate)
- Channel region:  $L$  ( $0.03\mu\text{m}$ – $1\mu\text{m}$ ),  $W$  ( $0.05\mu\text{m}$ – $100\mu\text{m}$ )

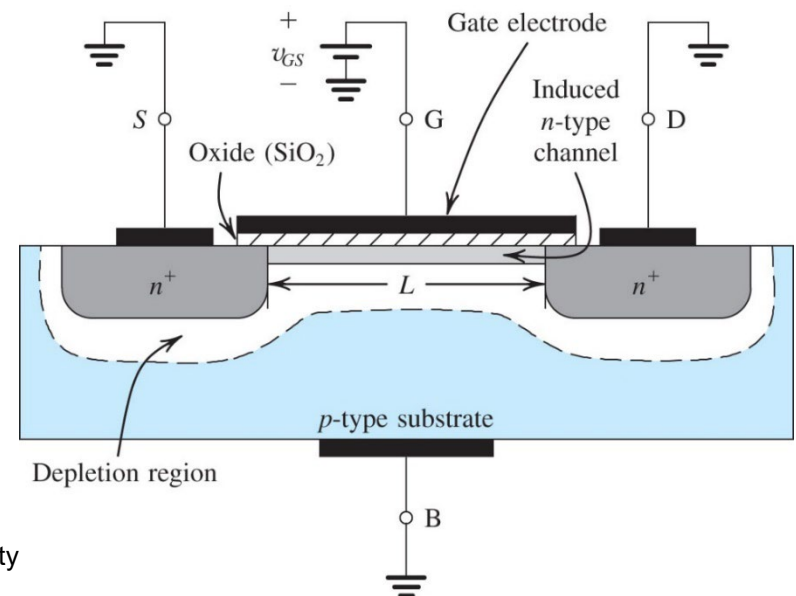


**Figure 5.1** Physical structure of the enhancement-type NMOS transistor: **(a)** perspective view; **(b)** cross section. Typically  $L = 0.03\ \mu\text{m}$  to  $1\ \mu\text{m}$ ,  $W = 0.05\ \mu\text{m}$  to  $100\ \mu\text{m}$ , and the thickness of the oxide layer ( $t_{ox}$ ) is in the range of 1 to 10 nm.

## • 5.1.3 Field-effect transistor (FET)

- Positive gate: repel holes and attract electrons from drain and source into the channel
- **Threshold voltage ( $V_t$ , 0.3V~1.0V)**: the value of  $V_{GS}$  to form a conducting channel
- Electric field:
  - Positive on the gate and negative in the channel form a field
  - The field determines the channel conductivity and the current flow through the channel

**Figure 5.2** The enhancement-type NMOS transistor with a positive voltage applied to the gate. An  $n$  channel is induced at the top of the substrate beneath the gate.



- 5.1.4 A small  $v_{DS}$ :  $i_D = [(u_n C_{ox}) (\frac{W}{L}) (v_{GS} - V_{tn})] v_{DS}$

$$\Rightarrow i_D = k_n v_{OV} v_{DS}$$

- Conductance  $g_{DS} = (u_n C_{ox}) (\frac{W}{L}) (v_{GS} - V_{tn})$

- $k'_n = u_n C_{ox}$ : process transconductance

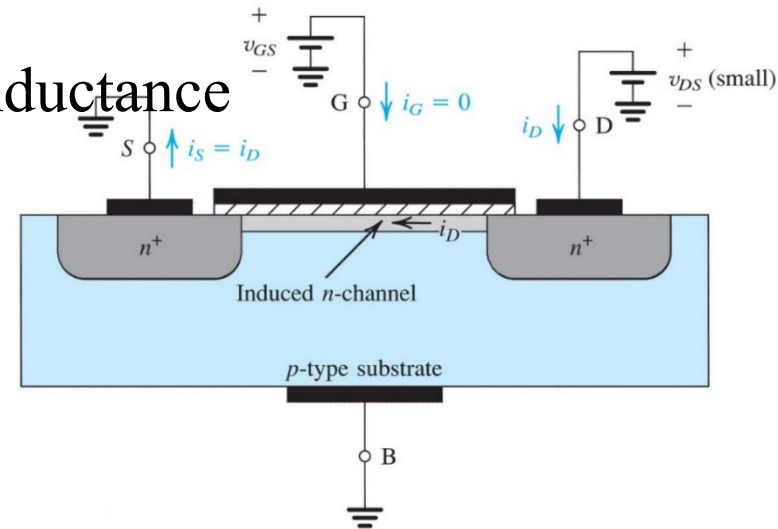
- $u_n$ : mobility of the electrons;

- $C_{ox}$ : oxide capacitance

- $k_n = k'_n (\frac{W}{L})$ : MOSFET transconductance

- $v_{OV} = v_{GS} - V_{tn}$ :

overdrive voltage -- determine  
the charge of the channel

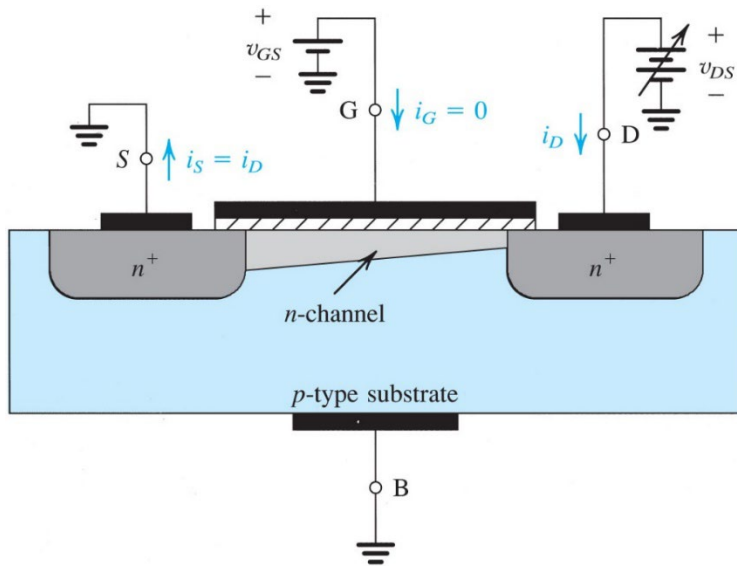


**Figure 5.3** An NMOS transistor with  $v_{GS} > V_t$  and with a small  $v_{DS}$  applied. The device acts as a resistance whose value is determined by  $v_{GS}$ . Specifically, the channel conductance is proportional to  $v_{GS} - V_t$ , and thus  $i_D$  is proportional to  $(v_{GS} - V_t) v_{DS}$ . Note that the depletion region is not shown (for simplicity).

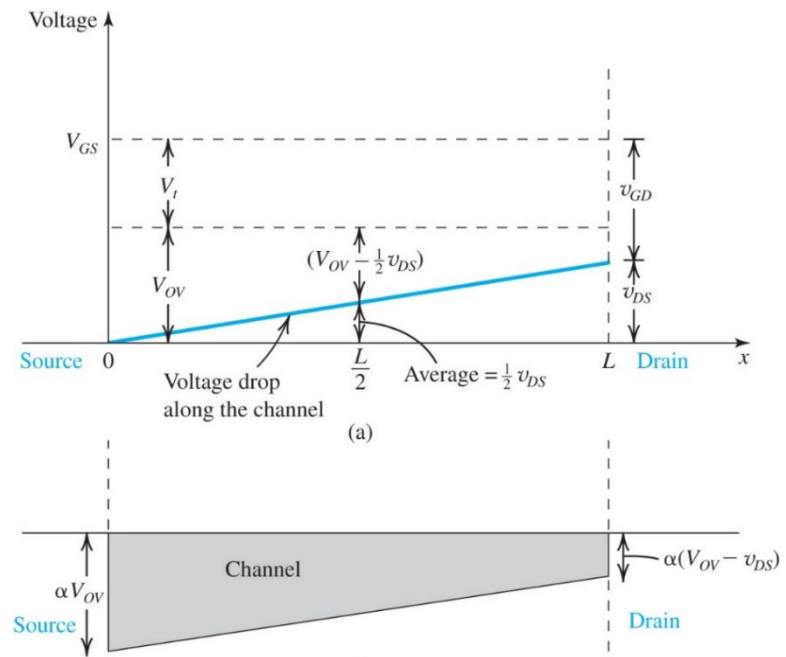
- 5.1.5  $v_{DS}$  increased but  $v_{DS} < V_{OV}$  :

$$i_D = k'_n \left( \frac{W}{L} \right) \left[ (v_{GS} - V_{tn}) - \frac{1}{2} v_{DS} \right] v_{DS} \Rightarrow i_D = k_n (v_{OV} - \frac{1}{2} v_{DS}) v_{DS}$$

- **Tapered shape** channel: deep at source (proportional to  $V_{OV}$ ) and shallow at drain (proportional to  $V_{OV} - v_{DS}$ )



**Figure 5.5** Operation of the enhancement-type NMOS transistor as  $v_{DS}$  is increased. The induced channel acquires a tapered shape, and its resistance increases as  $v_{DS}$  is increased. Here,  $v_{GS}$  is kept constant at a value  $> V_t$ ;  $v_{GS} = V_t + V_{OV}$ .



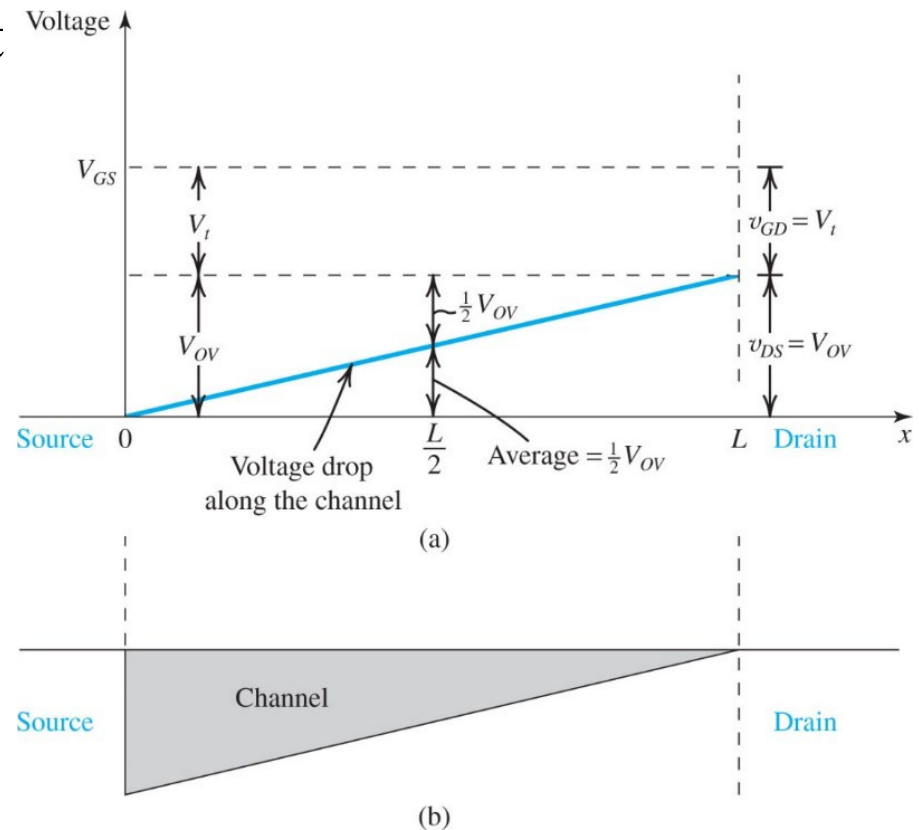
**Figure 5.6** (a) For a MOSFET with  $v_{GS} = V_t + V_{OV}$ , application of  $v_{DS}$  causes the voltage drop along the channel to vary linearly, with an average value of  $\frac{1}{2} v_{DS}$  at the midpoint. Since  $v_{DS} > V_t$ , the channel still exists at the drain end. (b) the channel shape corresponding to the situation in (a). While the depth of the channel at the source end is still proportional to  $V_{OV}$ , that at the drain end is proportional to  $V_{OV} - v_{DS}$

- 5.1.6  $v_{DS} \geq V_{OV}$ : channel pinch-off and current saturation,  $i_D = \frac{1}{2} k'_n \left(\frac{W}{L}\right) (v_{GS} - V_{tn})^2$

$$\Rightarrow i_D = \frac{1}{2} k_n v_{OV}^2$$

– Current remains constant

**Figure 5.8** Operation of MOSFET with  $v_{GS} = V_t + V_{OV}$ , as  $v_{DS}$  is increased to  $V_{OV}$ . At the drain end,  $v_{GD}$  decreases to  $V_t$  and the channel depth at the drain end reduces to zero (pinch-off). At this point, the MOSFET enters the saturation mode of operation. Further increasing  $v_{DS}$  (beyond  $V_{DSSat} = V_{OV}$ ) has no effect on the channel shape and  $i_D$  remains constant.



- Conclusion:

- $v_{GS} < V_{tn}$ : cut off

- $v_{GS} > V_{tn}$ : channel conducted

- A small  $v_{DS}$ :  $i_D = k_n v_{OV} v_{DS}$

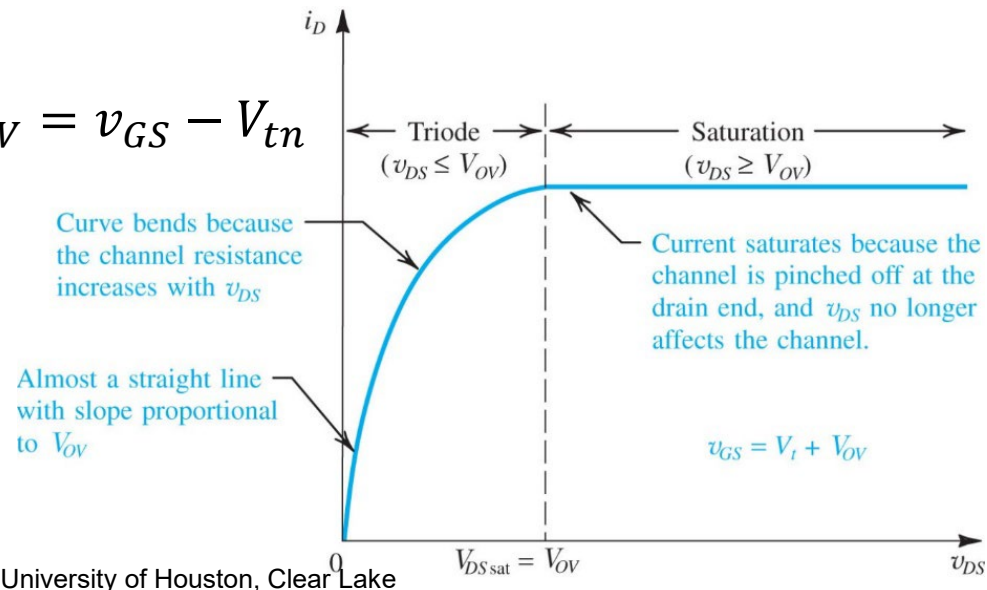
- $v_{DS}$  increased:  $i_D = k_n (v_{OV} - \frac{1}{2} v_{DS}) v_{DS}$

- $v_{DS} \geq V_{OV}$ : channel pinch-off and current saturation

$$i_D = \frac{1}{2} k_n v_{OV}^2$$

$$k'_n = \mu_n C_{ox}, k_n = k'_n \left( \frac{W}{L} \right), v_{OV} = v_{GS} - V_{tn}$$

**Figure 5.7** the drain current  $i_D$  versus the drain-to-source voltage  $v_{DS}$  for an enhancement-type NMOS transistor operated with  $v_{GS} = V_t + V_{OV}$ .



## • Example 5.1

Consider a process technology for which  $L = 0.4\mu\text{m}$ ,  $C_{ox} = \frac{\epsilon_{ox}}{t_{ox}} = 4.32 \times 10^{-3} \frac{\text{F}}{\text{m}^2}$  (hint:  $F = \frac{\text{A}\cdot\text{S}}{\text{V}}$ ),  $u_n = 450 \frac{\text{cm}^2}{\text{V}\cdot\text{s}}$ , and  $V_{tn} = 0.7\text{V}$ .

- (a) Find process transconductance  $k'_n$
- (b) For  $\frac{W}{L} = \frac{8\mu\text{m}}{0.8\mu\text{m}}$ , calculate  $V_{OV}$ ,  $V_{GS}$ ,  $V_{DSmin}$  needed to operate the transistor in saturation region with a dc current  $I_D = 100\mu\text{A}$

$$\text{(a) } k'_n = u_n C_{ox} = 4.32 \times 10^{-3} \frac{\text{F}}{\text{m}^2} \times 450 \frac{\text{cm}^2}{\text{V}\cdot\text{s}} = 4.32 \times 10^{-3} \frac{\text{A}\cdot\text{S}}{\text{V}\cdot\text{m}^2} \times 450 \times 10^{-4} \frac{\text{m}^2}{\text{V}\cdot\text{s}} = 1944 \times 10^{-7} \frac{\text{A}}{\text{V}^2} = 194.4 \frac{\mu\text{A}}{\text{V}^2}$$

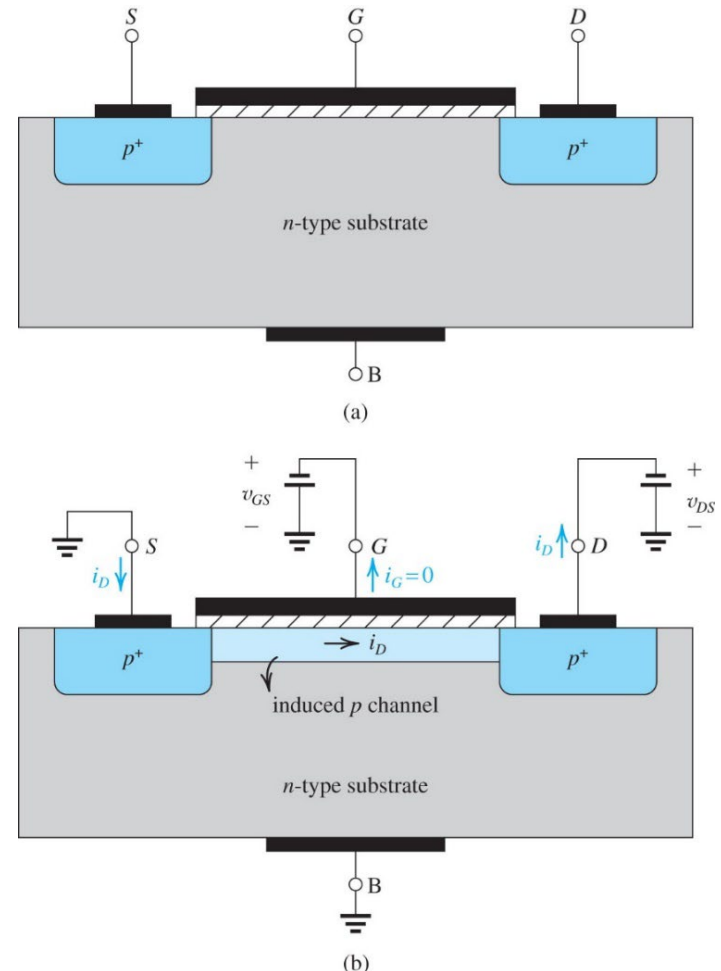
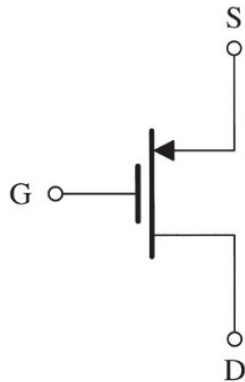
$$\text{(b) In saturation region, } i_D = \frac{1}{2} k'_n \left(\frac{W}{L}\right) V_{OV}^2 \quad (\text{Hint: } V_{OV} = V_{GS} - V_{tn})$$

$$V_{OV} = \sqrt{\frac{2i_D}{k'_n \left(\frac{W}{L}\right)}} = 0.32\text{V} \quad V_{GS} = V_t + V_{OV} = 1.02\text{V}$$

At the edge of saturation and triode,  $V_{DSmin} = V_{OV} = 0.32\text{V}$

## • 5.1.7 PMOS: P-Channel MOSFET

- $V_{SG} \geq |V_{tP}|$
- $k'_p = u_p C_{ox}$ 
  - $u_p$  is mobility of the holes
  - $u_p = 0.25u_n$  to  $0.5u_n$



**Figure 5.9** (a) Physical structure of the PMOS transistor. Note that it is similar to the NMOS transistor shown in Fig. 5.1(b) except that all semiconductor regions are reversed in polarity. (b) A negative voltage  $v_{GS}$  of magnitude greater than  $V_{tp}$  induces a  $p$  channel, and a negative  $v^{DS}$  causes a current  $i^D$  to flow from source to drain.

- Conclusion for PMOS:

- $v_{SG} < |V_{tp}|$ : cut off

- $v_{SG} > |V_{tp}|$ : channel conducted

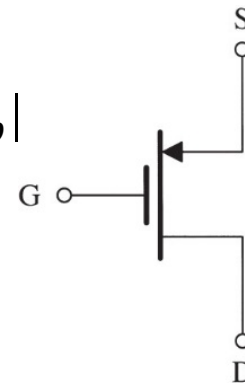
- A small  $v_{SD}$ :  $i_D = k_p v_{OV} v_{SD}$

- $v_{SD}$  increased:  $i_D = k_p (v_{OV} - \frac{1}{2} v_{SD}) v_{SD}$

- $v_{SD} \geq V_{OV}$ : channel pinch-off and current saturation

$$i_D = \frac{1}{2} k_p v_{OV}^2$$

$$k_p' = \mu_p C_{ox}, k_p = k_p' \left( \frac{W}{L} \right), v_{OV} = v_{SG} - |V_{tp}|$$



**Figure 5.7** the drain current  $i_D$  versus the drain-to-source voltage  $v_{SD}$  for an enhancement-type PMOS transistor operated with  $v_{SG} = V_{tp} + V_{OV}$ .

## • Example 5.2

For a  $0.18\text{-}\mu\text{m}$  fabrication process with  $W = 2\mu\text{m}$ . The process is specified to have  $C_{ox} = 8.6 \frac{\text{fF}}{\mu\text{m}^2}$ , (hint:  $1\text{fF} = 10^{-15}\text{F}$ ,  $\text{F} = \frac{\text{A}\cdot\text{S}}{\text{V}}$ ),  $u_n = 450\text{cm}^2/\text{V}\cdot\text{s}$ , and  $V_{tn} = 0.5\text{V}$ .

(a) Find  $V_{GS}$  and  $V_{DS}$  that result in the MOSFET operating at the edge of saturation with  $I_D = 100\mu\text{A}$ .

$$k'_n = u_n C_{ox} = 450 \times 10^8 \frac{\mu\text{m}^2}{\text{V}\cdot\text{s}} \times 8.6 \times 10^{-15} \frac{\text{F}}{\mu\text{m}^2} = 387 \frac{\mu\text{A}}{\text{V}^2}$$

$$k_n = k'_n \left( \frac{W}{L} \right) = 387 \times \frac{2}{0.18} = 4.3 \times 10^3 \frac{\mu\text{A}}{\text{V}^2}$$

(a) At the edge of saturation,  $I_D = \frac{1}{2} k_n V_{ov}^2$ ,

$$100 = \frac{1}{2} \times 4.3 \times 10^3 \times V_{ov}^2, \Rightarrow V_{OV} = 0.22\text{V}$$

Thus  $V_{DS} = V_{OV} = 0.22\text{V}$  and  $V_{GS} = V_{OV} + V_{tn} = 0.72\text{V}$

## • Example 5.2

For a  $0.18\text{-}\mu\text{m}$  fabrication process with  $W = 2\mu\text{m}$ . The process is specified to have  $C_{ox} = 8.6 \frac{\text{fF}}{\mu\text{m}^2}$ , (hint:  $1\text{fF} = 10^{-15}\text{F}$ ),  $\mu_n = 450\text{cm}^2/\text{V} \cdot \text{s}$ , and  $V_{tn} = 0.5\text{V}$ .

(b) If  $V_{GS}$  is kept constant, find  $V_{DS}$  that result in  $I_D = 50\mu\text{A}$ .

(b) With  $V_{GS} = 0.72\text{V}$  and  $I_D$  reduced from the value obtained at the edge of saturation ( $I_D = 100\mu\text{A}$ ), the MOSFET will be working in triode region.

In triode region,  $I_D = k_n (V_{OV} - \frac{1}{2}V_{DS})V_{DS}$ ,

$$50 = 4.3 \times 10^3 \times (0.22 - \frac{1}{2}V_{DS})V_{DS},$$

$$\Rightarrow V_{DS}^2 - 0.44V_{DS} + 0.023 = 0$$

Thus  $V_{DS} = 0.06\text{V}$  and  $V_{DS} = 0.39\text{V}$

If  $V_{DS} = 0.39\text{V}$ , the transistor is in saturation region, so  $V_{DS} = 0.06\text{V}$

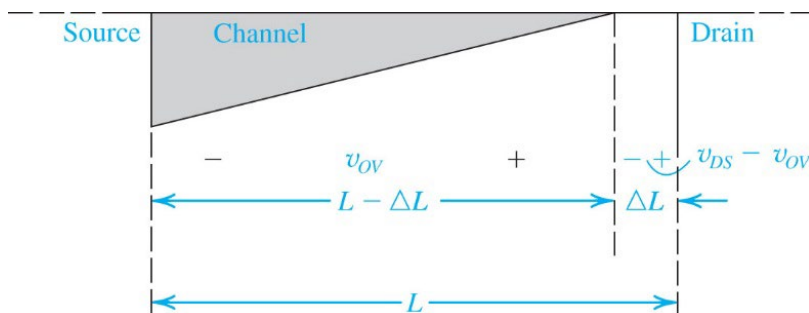
## • 5.2.4 Finite output resistance in saturation

### – Channel-length modulation

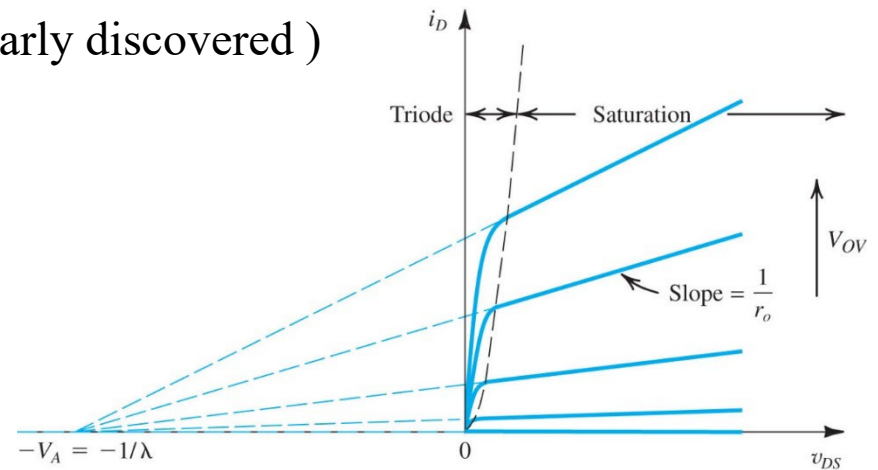
- As  $v_{DS}$  increases, the channel pinch-off point is moved slightly away from the drain, toward the source (channel length reduced).
- $i_D$  is inversely proportional to channel length, so increases with  $v_{DS}$

$$- i_D = \frac{1}{2} k'_n \left( \frac{W}{L} \right) (V_{GS} - V_{tn})^2 (1 + \lambda v_{DS})$$

- $\lambda$ : device parameter with unit of reciprocal volts ( $V^{-1}$ )
- $V_A = \frac{1}{\lambda}$ , early voltage (J. M. Early discovered )



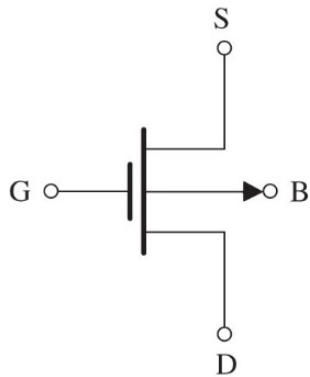
**Figure 5.16** Increasing  $v_{DS}$  beyond  $v_{DSsat}$  causes the channel pinch-off point is moved slightly away from the drain, thus reducing the effective channel length (by  $\Delta L$ ).



**Figure 5.16** Effect of  $v_{DS}$  on  $i_D$  in the saturation region. The MOSFET parameter  $V_A$  depends on the process technology and, for a given process, is proportional to the channel length  $L$ .

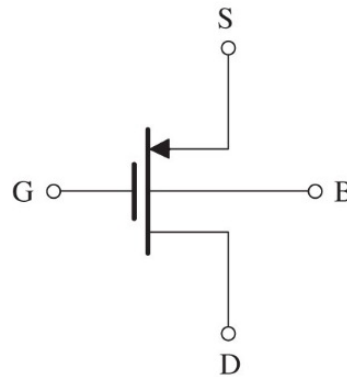
- 5.2.5 P-channel MOSFET symbols and characteristics

$$I_D = \frac{1}{2} k'_p \left( \frac{W}{L} \right) (V_{SG} - |V_{tp}|)^2 (1 + |\lambda| V_{SD})$$



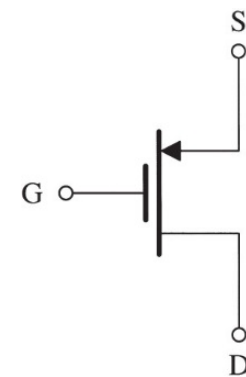
(a)

**Figure 5.19 (a)** Circuit symbol for the *p*-channel enhancement-type MOSFET.



(b)

**Figure 5.19 (b)** Modified symbol with an arrowhead on the source lead.



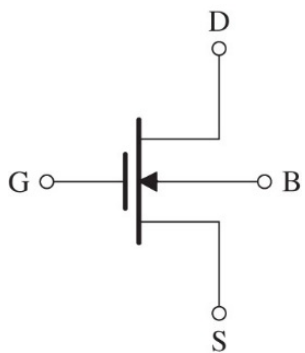
(c)

**Figure 5.19 (c)** Simplified circuit symbol for the case where the source is connected to the body.

# 5.2 $i_D - v_{DS}$ characteristics

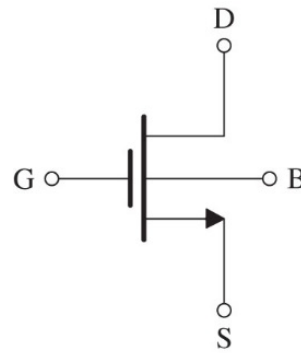
## • 5.2.1 Circuit symbol

- (a) isolation (spacing between the vertical lines) and polarity (arrowhead)
- (b) current from drain to source (c) simplified symbol



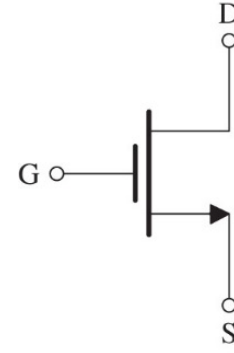
(a)

**Figure 5.11 (a)** Circuit symbol for the  $n$ -channel enhancement-type MOSFET



(b)

**Figure 5.11 (b)** Modified circuit symbol with an arrowhead on the source terminal to distinguish it from the drain and to indicate device polarity (i.e.,  $n$  channel).

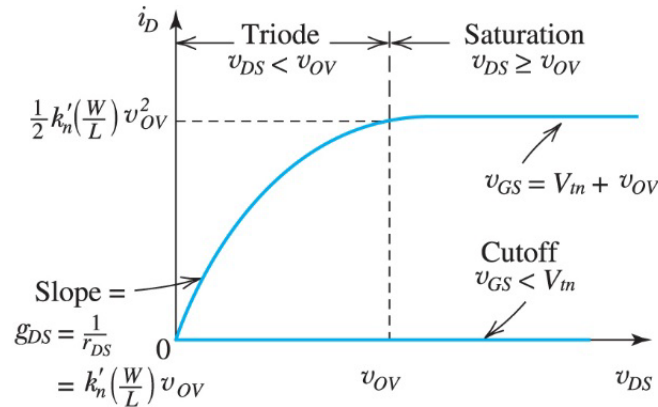
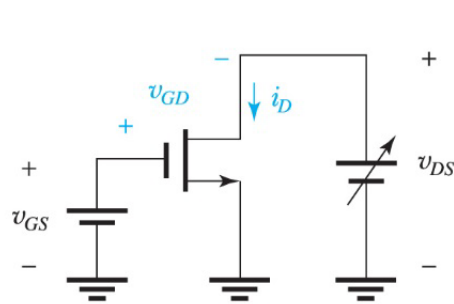


(c)

**Figure 5.11 (c)** Simplified circuit symbol to be used when the source is connected to the body or when the effect of the body on device operation is unimportant.

# • 5.2.2 The NMOS $i_D - v_{DS}$ characteristics

**Table 5.1** Regions of Operation of the Enhancement NMOS Transistor



- $v_{GS} < V_{in}$  : no channel; transistor in cutoff;  $i_D = 0$
- $v_{GS} = V_{in} + v_{OV}$  : a channel is induced; transistor operates in the triode region or the saturation region depending on whether the channel is continuous or pinched off at the drain end;

### Triode Region

Continuous channel, obtained by:

$$v_{GD} > V_{in}$$

or equivalently:

$$v_{DS} < v_{OV}$$

Then,

$$i_D = k'_n \left( \frac{W}{L} \right) \left[ (v_{GS} - V_{in}) v_{DS} - \frac{1}{2} v_{DS}^2 \right]$$

or equivalently

$$i_D = k'_n \left( \frac{W}{L} \right) \left( v_{OV} - \frac{1}{2} v_{DS} \right) v_{DS}$$

### Saturation Region

Pinched-off channel, obtained by:

$$v_{GD} \leq V_{in}$$

or equivalently:

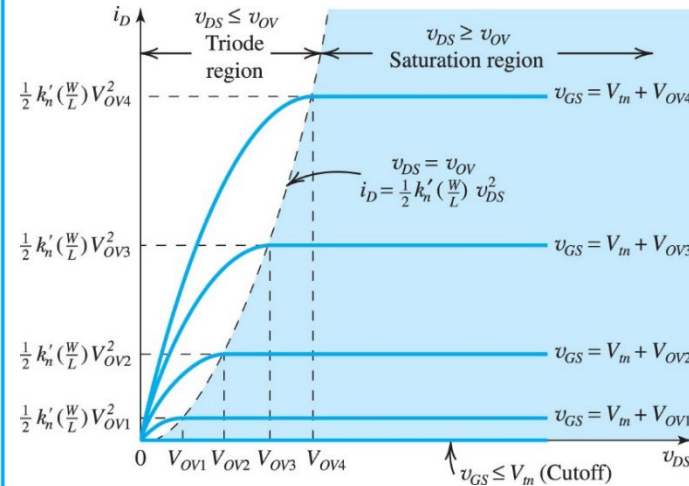
$$v_{DS} \geq v_{OV}$$

Then

$$i_D = \frac{1}{2} k'_n \left( \frac{W}{L} \right) (v_{GS} - V_{in})^2$$

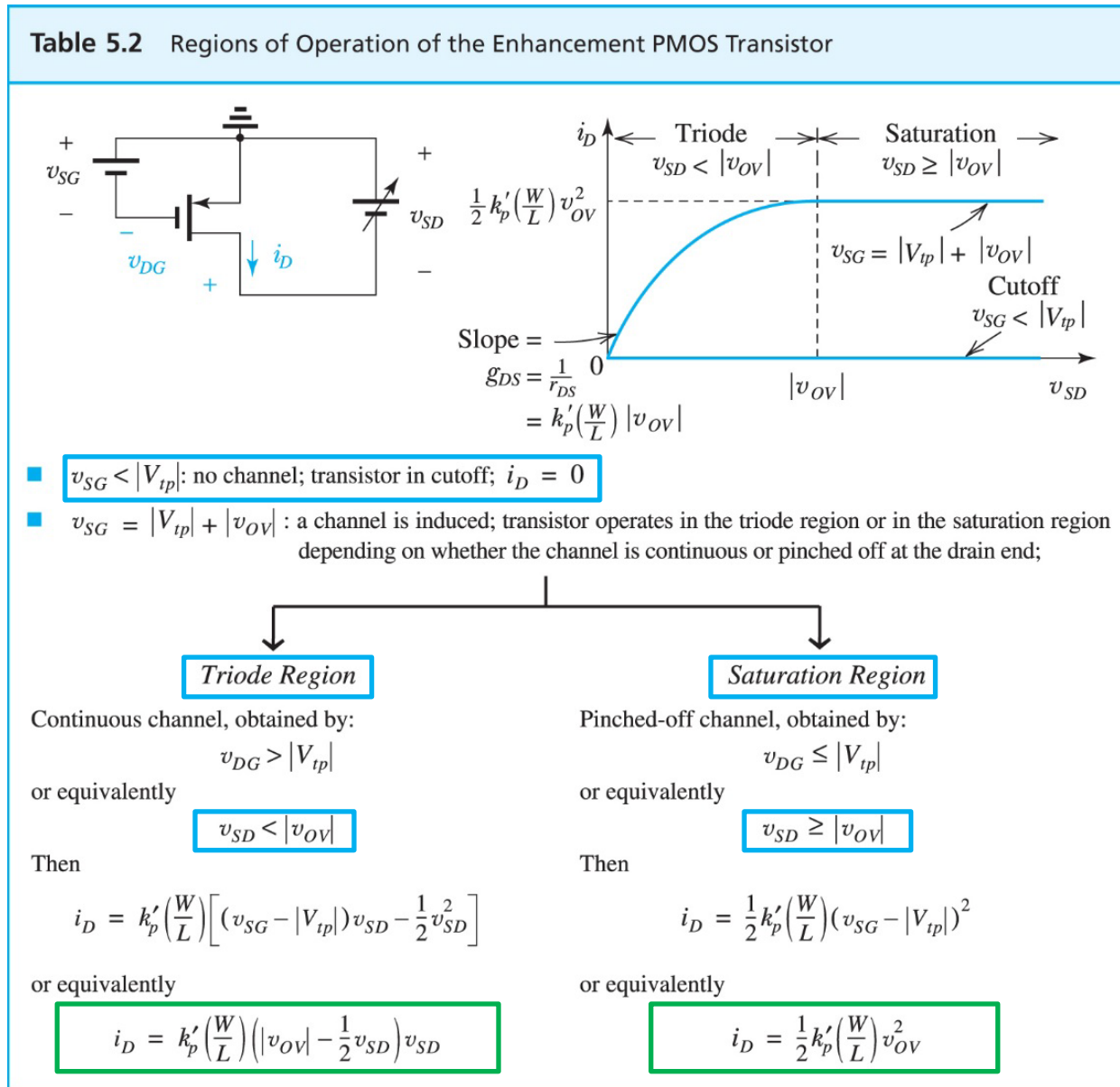
or equivalently

$$i_D = \frac{1}{2} k'_n \left( \frac{W}{L} \right) v_{OV}^2$$



**Figure 5.13** The  $i_D - v_{DS}$  characteristics for an enhancement-type NMOS transistor

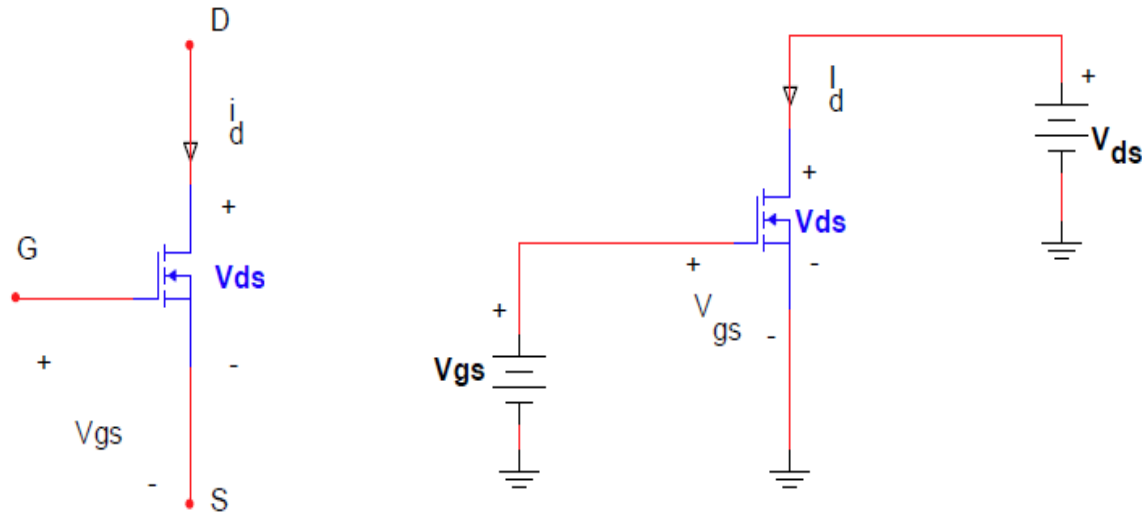
- P-channel MOSFET symbols and characteristics





# • Experiment 7

Set up the following circuit with an enhancement nMOSFET (**2N7000**).



**Do a quick measurement** for all cases below.

- c) Identify the triode and saturation regions in the graph
- d) Estimate the threshold voltage,  $V_t$
- e) Estimate  $k_n$

Briefly explain and comment your results.

# 5.3 MOSFET circuit at DC

- In which mode is the transistor operating?

## Top-Bottom-Threshold rule (TBT)

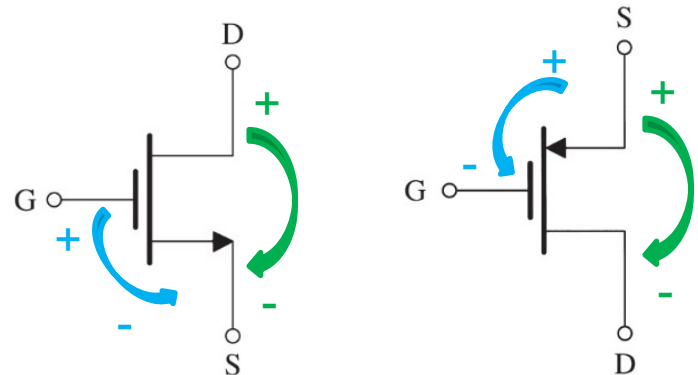
- First TBT (GS/SG VS.  $V_t$ )?

- $TB > |V_t|$  ( $V_{GS} > |V_{tn}|$  for NMOS,  $V_{SG} > |V_{tp}|$  for PMOS) => **Conducting**
- $TB < |V_t|$  => **Cutoff**

- Second TBT (DS/SD VS.  $V_{OV}$ )?

- $TB > V_{OV}$  ( $V_{DS} \geq V_{OV}$  for NMOS,  $V_{SD} \geq V_{OV}$  for PMOS) => **Saturation**
- $TB < V_{OV}$  => **Triode**

$$V_{OV} = V_{GS} - V_{tn} \text{ for NMOS}$$
$$V_{OV} = V_{SG} - |V_{tp}| \text{ for PMOS}$$



- Analysis procedure

- Find conduction (**GS/SG VS.  $V_t$** : 1<sup>st</sup> TBT rule)

- If conducting -> **assume in saturation mode first**
- If not conducting, in cutoff

- Proceeds all currents and voltages

- Find saturation (**DS/SD VS.  $V_{OV}$** : 2<sup>nd</sup> TBT rule)

- In saturation
- If not saturated, in triode mode -> redo the analysis

Another solution to find saturation:

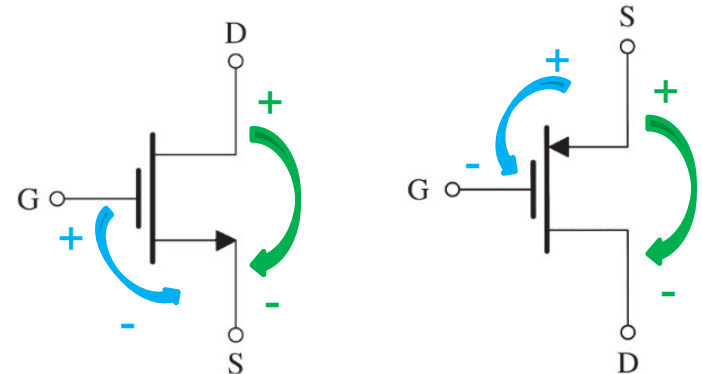
$$V_{DS} > V_{OV} \Rightarrow V_D - V_S > V_G - V_S - V_{tn} \Rightarrow$$

$$V_{DG} > -V_{tn} \quad (V_{DG} \geq 0)$$

For PMOS,

$$V_{SD} > V_{OV} \Rightarrow V_S - V_D > V_S - V_G - |V_{tp}| \Rightarrow$$

$$V_{GD} > -|V_{tp}| \quad (V_{GD} \geq 0)$$



## • Example 5.3

Design the circuit: determine the values of  $R_D$  and  $R_S$  so that the transistor operates at  $I_D = 0.4\text{mA}$  and  $V_D = 0.5\text{V}$ . The NMOS transistor has  $V_t = 0.7\text{V}$ ,  $u_n C_{ox} = 100\mu\text{A}/\text{V}^2$ ,  $L = 1\mu\text{m}$ , and  $W = 32\mu\text{m}$ . Neglect the channel-length modulation effect ( $\lambda = 0$ ).

$$R_D = \frac{2.5 - V_D}{I_D} = \frac{2.5 - 0.5}{0.4} = 5\text{k}\Omega$$

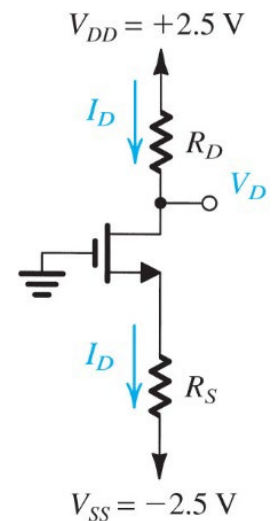
Glancing  $V_D > V_G$  ( $V_{DS} > V_{GS}$ ), so the transistor in saturation.

$$k_n = u_n C_{ox} \left( \frac{W}{L} \right) = 100 \times \frac{32}{1} = 3.2 \frac{\text{mA}}{\text{V}^2}$$

$$I_D = \frac{1}{2} k_n V_{OV}^2 \Rightarrow 0.4 = \frac{1}{2} \times 3.2 \times V_{OV}^2 \Rightarrow V_{OV} = 0.5\text{V}$$

$$V_{GS} - V_t = 0.5\text{V}, \text{ thus } V_G - V_S - V_t = 0.5\text{V} \Rightarrow V_S = -1.2\text{V}$$

$$R_S = \frac{-1.2\text{V} - (-2.5\text{V})}{I_D} = 3.25\text{k}\Omega$$



- Example 5.4 (diode-connected transistor)

Find the  $i - v$  relationship in terms of the MOSFET parameters

$k_n = k'_n \left(\frac{W}{L}\right)$  and  $V_{tn}$ . Neglect the channel-length modulation ( $\lambda = 0$ ).

Note that this two-terminal device is known as a diode-connected transistor.

Since  $V_D = V_G$  implies operation in the saturation region.

$$I_D = \frac{1}{2} k'_n \left(\frac{W}{L}\right) (V_{GS} - V_{tn})^2$$

$$\text{So } I_D = \frac{1}{2} k_n (v - V_{tn})^2$$

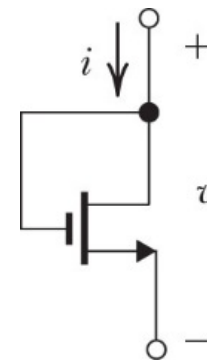


Figure 5.22

- Example 5.5

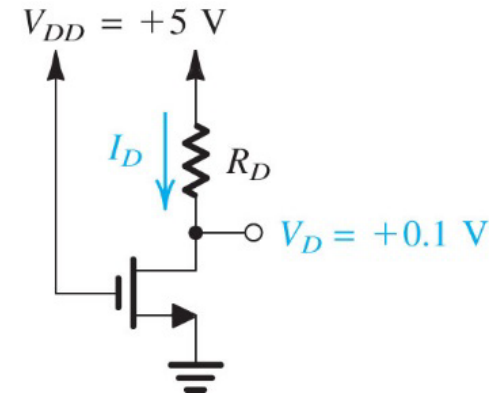
Design a circuit (Find  $R_D$ ) to establish a drain voltage of  $V_D = 0.1V$ . What is the effective resistance between drain and source at this operating point ( $r_{DS}$ )? Let  $V_{tn} = 1V$ ,  $k'_n(W/L) = 1mA/V^2$

Since  $V_{DS}(0.1V) < V_{OV}$  ( $V_{GS} - V_{tn} = 5 - 1 = 4V$ ), the transistor operates in triode region.

$$I_D = k'_n \left( \frac{W}{L} \right) \left[ V_{OV} - \frac{1}{2} V_{DS} \right] V_{DS} = 1 \times (4 - 0.05) \times 0.1 = 0.395mA$$

$$R_D = \frac{5V - 0.1V}{I_D} = 12.4k\Omega$$

$$r_{DS} = \frac{0.1V}{I_D} = 253\Omega$$



# • Example 5.6

Analyze the circuit to determine the voltages at all nodes and the currents through all branches. Let  $V_{tn} = 1V$ ,  $k'_n(W/L) = 1 mA/V^2$ . Neglect the channel-length modulation effect ( $\lambda = 0$ ).

$$V_G = \frac{1}{2} V_{DD} = 5V$$

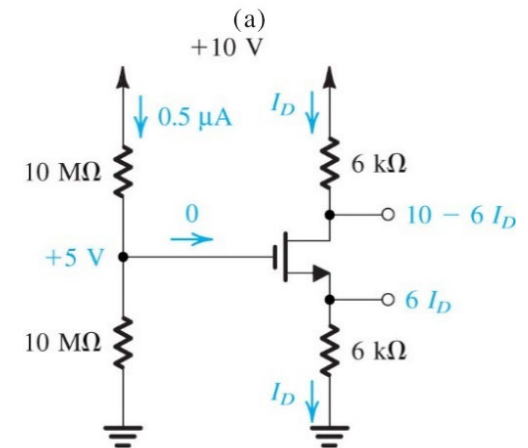
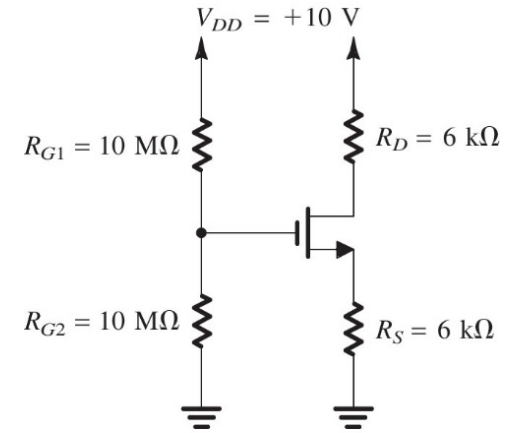
Since  $V_G = 5V$  and  $V_S$  is grounded through a  $6k\Omega$  resistor, the transistor is turned on. Assume that the transistor operates in saturation region.

$$V_S = I_D \times 6k\Omega$$

$$I_D = \frac{1}{2} k'_n(W/L) (V_{GS} - V_{tn})^2 = \frac{1}{2} \times 1 \times (5 - 6I_D - 1)^2$$

$$\Rightarrow 18I_D^2 - 25I_D + 8 = 0$$

This equation yields two values for  $I_D$ :  $0.5mA$  and  $0.89mA$



**Figure 5.24** (a) Circuit for Example 5.6. (b) The circuit with some of the analysis details shown

## • Example 5.6 Cont.

Analyze the circuit to determine the voltages at all nodes and the currents through all branches. Let  $V_{tn} = 1V$ ,  $k'_n(W/L) = 1 \text{ mA/V}^2$ . Neglect the channel-length modulation effect ( $\lambda = 0$ ).

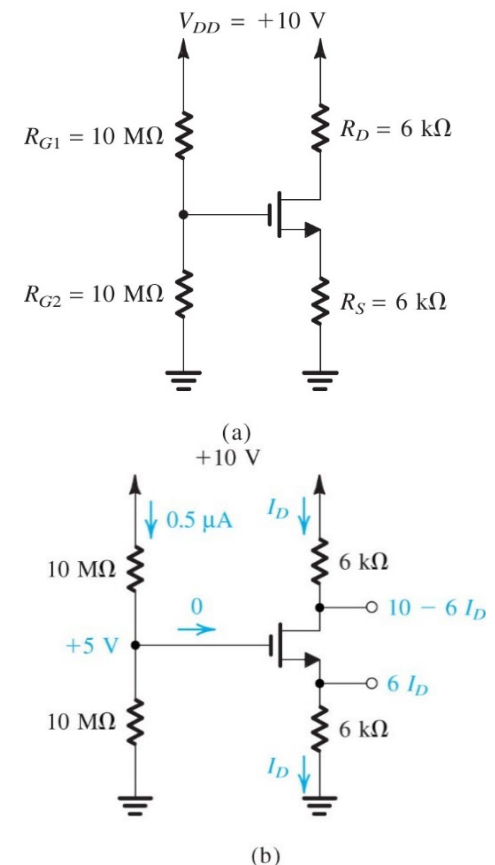
① If  $I_D = 0.89\text{mA}$ ,  $V_S = I_D \times 6\text{k}\Omega = 5.34\text{V} > V_G$ , doesn't make physical sense, should cutoff the transistor.

② Thus,  $I_D = 0.5\text{mA}$

$$V_S = I_D \times 6 = 3\text{V}, V_D = 10 - I_D \times 6 = 7\text{V}$$

Since  $V_{GS} = 5\text{V} - 3\text{V} = 2\text{V}$ ,  $V_{DS} = 7\text{V} - 3\text{V} = 4\text{V}$

$V_{DS} > V_{GS} - V_{tn}$ , in saturation region.



**Figure 5.24** (a) Circuit for Example 5.6. (b) The circuit with some of the analysis details shown.

## • Example 5.7

- a) Find  $R_{G1}$ ,  $R_{G2}$ , and  $R_D$  so that the transistor operates in saturation with  $I_D = 0.5\text{mA}$ ,  $V_D = 3\text{V}$ . Let the PMOS have  $V_{tp} = -1\text{V}$ ,  $k'_p(W/L) = 1\text{mA/V}^2$ .
- b) What is the largest value that  $R_D$  can have while the transistor remains in the saturation mode? Neglect the channel-length modulation effect ( $\lambda = 0$ ).

$$(a) I_D = \frac{1}{2}k'_p \left(\frac{W}{L}\right) V_{OV}^2 \Rightarrow V_{OV} = 1\text{V} \Rightarrow V_{SG} = V_{OV} + |V_{tp}| = 2\text{V}$$

$$\text{Thus } V_S - V_G = 2\text{V} \Rightarrow V_G = 5\text{V} - 2\text{V} = 3\text{V}$$

This can be achieved by appropriate selection of

$$R_{G1} = 2\text{M}\Omega, R_{G2} = 3\text{M}\Omega$$

$$R_D = \frac{V_D}{I_D} = \frac{3}{0.5} = 6\text{k}\Omega$$

$$(b) \text{ At the edge, } V_{SD} = V_S - V_D = |V_{OV}| = 1\text{V}$$

$$V_{Dmax} = V_S - |V_{OV}| = 4\text{V} \text{ thus } R_{Dmax} = \frac{V_{Dmax}}{I_D} = 8\text{k}\Omega$$

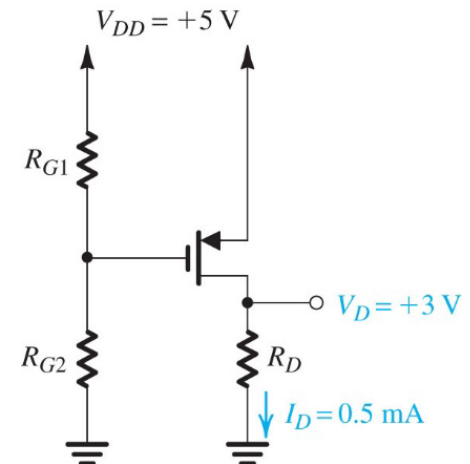


Figure 5.25 Circuit for Example 5.7.

# HW5

- Problems
  - PP.294, 5.18 – Current-Voltage Characteristics #1
  - PP.297, 5.38 – Current-Voltage Characteristics #2
  - PP.299, 5.44 – MOSFET Circuit at DC #1
  - PP.299, 5.49 – MOSFET Circuit at DC #2
  - PP.300, 5.54 – MOSFET Circuit at DC #3
- Submission requirement:
  - Add the cover page!!!
  - Print the HW5.pdf out and answer all the questions
- HW5 Due: TBA (Late assignments: 40% deduction. )