Chisel and IC Projects Structuring

Xiaokun Yang

9/26/2024

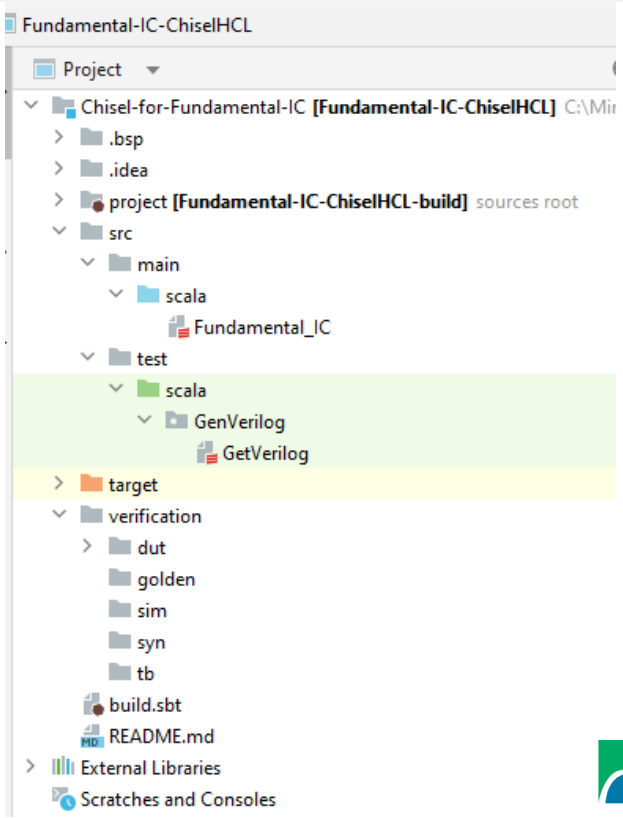
1. Project directory

1.1 Chisel related

src-main: all the Chisel designs are located in main-scala

src-test: the Chisel generation is located in test-scala-GenVerilog

verification-dut: all the generated Verilog is located in verification-dut



1. Project directory

1.2. Verilog design and simulation

In verification folder, it shows the design and verification env

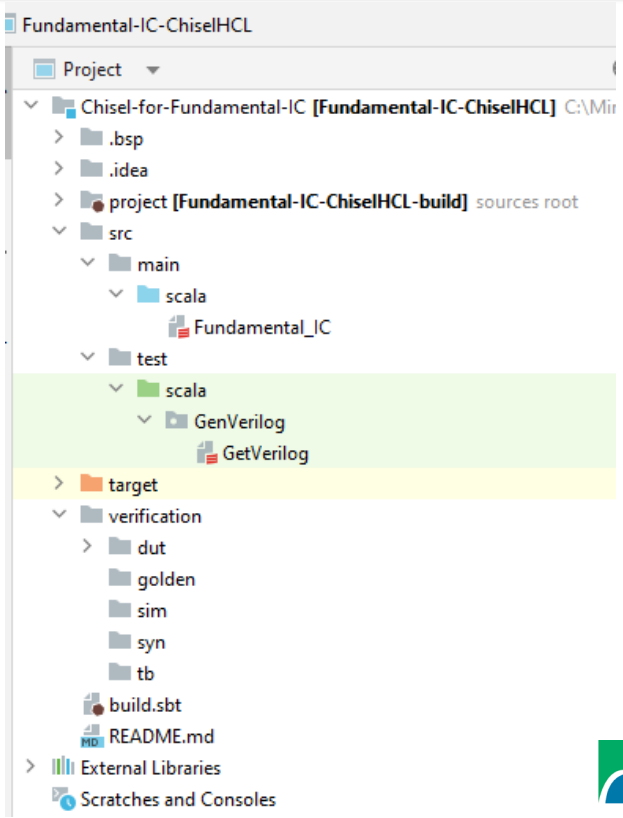
dut: design-under-test (Verilog/SystemVerilog designs)

golden: randomized input and golden output files

sim: run script for ModelSim simulator

syn: synthesis & implementation results for Vivado

tb: testbench



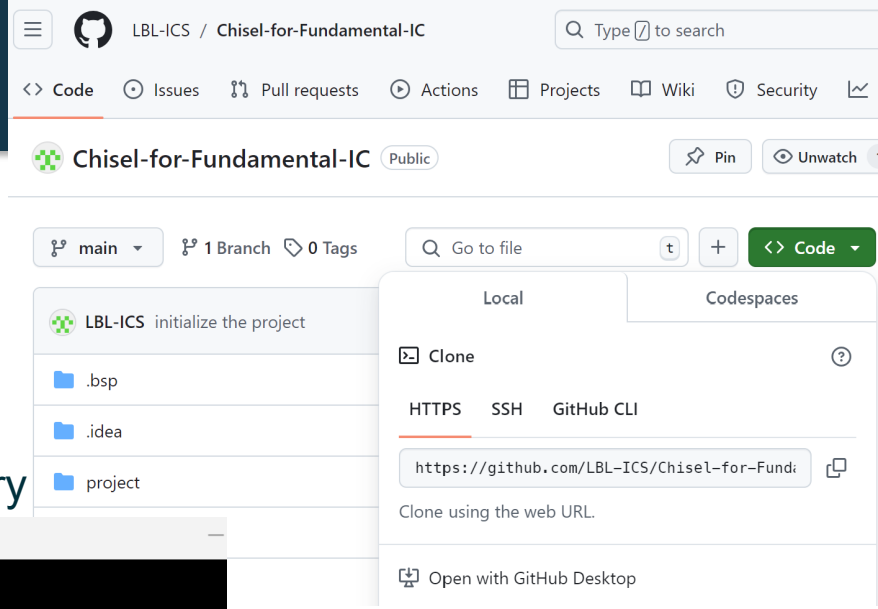
2. Project organization

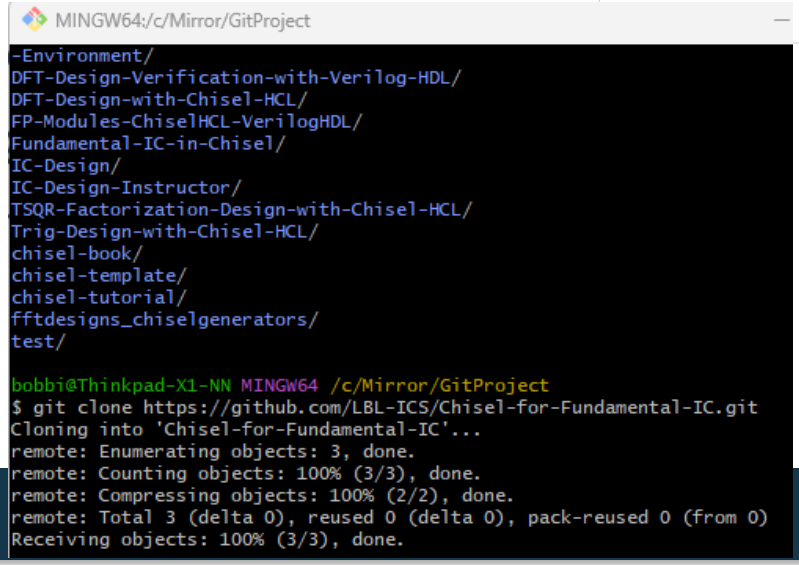
Git repository for project

a. Create a git repository

b. Locate to your local directory and open Gitbash

Clone the git repository to your local project directory





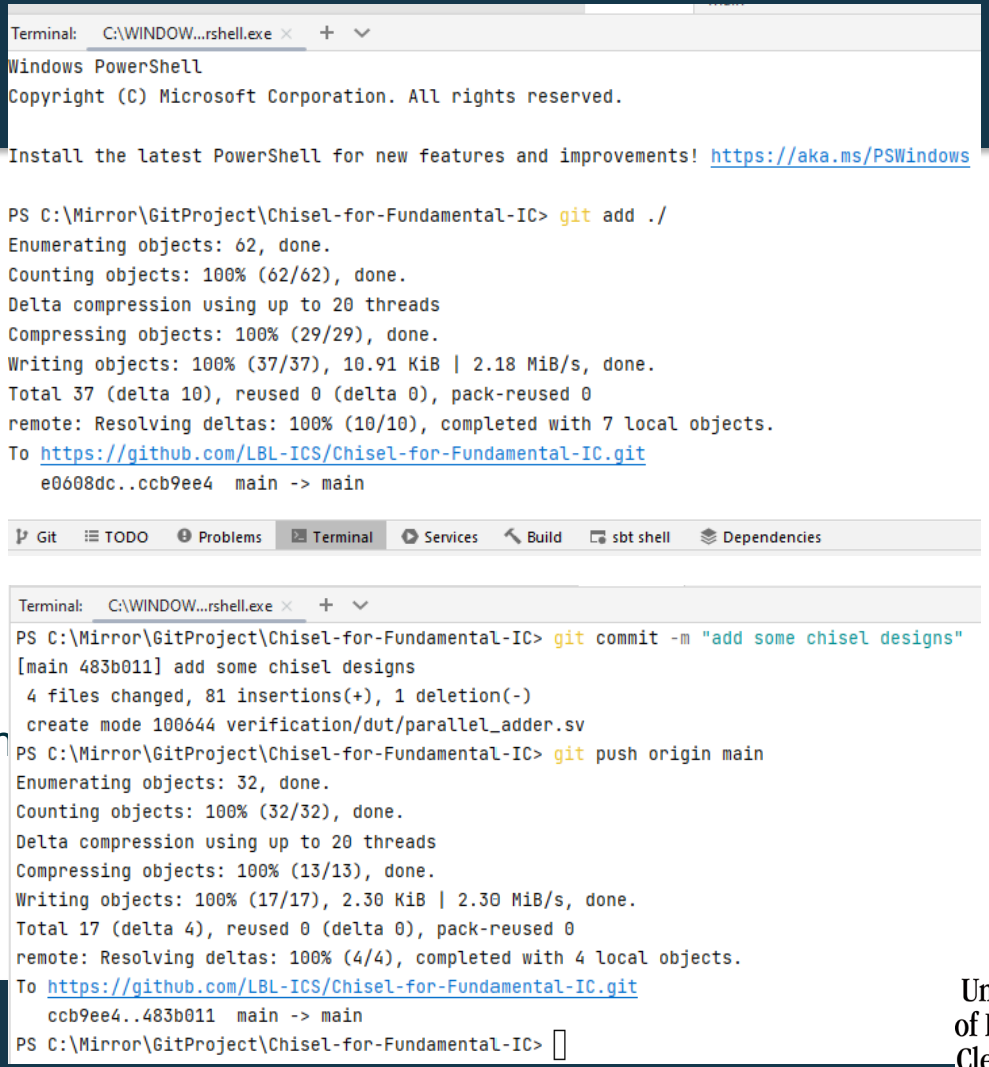
2. Project organization

c. Update your project

Locate to the terminal in Intellij, then

- git add ./
- git commit –m “your commit”
- git push –u origin main

Note: we use Git repository as the version control tool to maintain and organ projects. whenever you want to release your project, update to Git!



References

1. Chisel Design – XY. Pdf
2. Chisel Env Setup – XY. pdf
3. Chisel Designs for Fundamental IC, Git repository: https://github.com/LBL-ICS/Chisel-for-Fundamental-IC.git
4. Xiaokun Yang, “Integrated Circuit Design: IC Design Flow and Project-Based Learning”, CRC Press -Taylor & Francis Group, ISBN: 978-1-032-03079-1 (ebook ISBN: 978-1-003-18708-0), First edition
5. Chisel Bootcamp
6. Chisel3 Cheat sheet
7. Chisel textbook, version 5