Xiaokun Yang, Ph.D.
Associate Professor, UH-CL
Affiliate Faculty, Berkeley Lab

CONTACT INFO

UHCL Email: yangxia@uhcl.edu
Berkeley Lab Email: xiaokunyang@lbl.gov
Personal Web: http://sceweb.uhcl.edu/xiaokun
Google Scholar: https://scholar.google.com/citations?hl=en&user=GQw5udEAAAAJ

RESEARCH INTERESTS

- Hardware Design Generation on Neural Networks
- Hardware Acceleration on Quantum Circuit Simulation
- ASIC/FPGA/SoC Acceleration on Scientific Computing and HPC

EDUCATION

Florida International University, Miami, FL 2016
Ph.D., Computer Engineering
- Dissertation: *A High Performance AES-Encrypted On-Chip Bus Architecture for Internet-of-Things (IoT) System-on-Chips (SoC)*
- Advisor: Jean H. Andrian, Ph.D

Florida International University, Miami, FL 2008
M.S., Computer Engineering
- Thesis: *USB 2.0 Host Controller Design and Verification*
- Advisor: Jean H. Andrian, Ph.D

Beihang University, Beijing, China 2007
M.S., Software Engineering
- Advisor: Jinming Dong, Ph.D

Beihua University, Jilin, China 2004
B.S., Electrical and Computer Engineering

ACADEMIA EXPERIENCE

Associate Professor 2021 – Present
Computer Engineering
University of Houston Clear Lake **(UHCL)**

NSF REU Program Director 2024 – 2027
NSF REU Program (WSU-UHCL)
University of Houston Clear Lake **(UHCL)**

Affiliate Faculty Aug. 2022 – Present
Computational Research Division
Lawrence Berkeley National Laboratory **(LBNL)**

Assistant Professor 2016 – 2021
Computer Engineering
University of Houston Clear Lake **(UHCL)**

INDUSTRY EXPERIENCE

Sr. ASIC Design/Layout Engineer 2011 – 2012
GPU, Advanced Micro Devices **(AMD)**

Chip tape-out experiences : AMD CPUs/GPUs/APUs – Kabini, Kaveri, Bonaire, Kryptos, and Samara

Sr. ASIC Verification Engineer 2009 – 2010
WLAN, China Electronics Corp. (CEC)
Chip tape-out experiences : 802.11 a/b/g/n MIMO Mixed-Signal SoCs – CEC TL3 and TL5

ASIC Design Engineer 2007 – 2008
SoC Group, PowerLayer MicroSystems Corp. (PLM)
Chip tape-out experiences : PLM High-Definition TV (HDTV) SoCs – PLM3K and PLM5K

Honors, Awards, and Certificates

Research Grant (Awarded):

- Subawardee, (UHCL PI), *Department of Energy (DOE) ASCR 24-3210, Thrust-E: Basic research topics: Algorithm-Driven Codesign of Specialized Architectures for Energy-Efficient HPC.* $319,998 ($32,000,000 in total), Awarded. 2024-2028
- Co-PI, (UHCL PI), *NSF 2512983, Collaborative Research: Elements: Computational Storage Virtualization for Accelerating Data-Driven Scientific Applications on Supercomputers.* $120,621, ($400,000 in total), 2025-2028
- Co-PI, (UHCL PI), *NSF 2243981, Collaborative Research: REU Site: Advancing Data-Driven Deep Coupling of Computational Simulations and Experiments.* $46,706 ($450,623 in total), Awarded. 2024-2027
- PI, *Distinguished Professorship, UHCL Computer Science and Engineering, Bridging Classical IC Design and Quantum Circuit Simulation: A Parameterized and Scalable Hardware Emulation Framework.* $29,649, Awarded. 2025-2028
- NSF HSI Travel Grant, "Developing a High-Quality Academic Environment for Broadening Participation of Hispanic Students in Computing", UNT, Jan 23 2026, $2,000, Awarded. 2025
- PI, NSF Travel Grant, NSF CISE Research Expansion (RE) Aspiring PI Workshop, $1,500, Awarded. 2025
- PI, NSF Travel Grant, NSF CISE MSI Aspiring PI workshop, $1,300, Awarded. 2024
- PI, Berkeley Lab Fellowship, Collaborative Research: Hardware Accelerator Design on Density Functional Theory, $37,800, Awarded, DOE SU 2024
- PI, Berkeley Lab Fellowship, Collaborative Research: Hardware Accelerator Design on TSQR Factorization, $37,800, Awarded, DOE SU 2023
- PI, DOE VFP, Collaborative Research: Hardware Accelerator Design on 3D Fourier Transform,$25,900, Awarded, DOE SU 2022
- Research Advisor, Integrated Circuit Design and Verification, NSF HSI - ELPSG, $20,000, Awarded, UHCL 2022-2023
- Research Advisor, Hardware Generator Design and Verification, Department of Education (DoE) Pathway, $20,000, Awarded, UHCL 2022-2023
- PI, Center of Faculty Development Funds, $1,500.00, Awarded, UHCL 2021
- PI, Faculty Research and Support Funds (FRSF) $5,470.00, Awarded, UHCL 2021
- PI, Xilinx University Program, $1,600.00, Awarded, Xilinx 2020
- PI, Faculty Development Funds (FDF), $8,000.00, Awarded, UHCL 2017-2019
- PI, Faculty Research and Support Funds (FRSF) $5,730.00, Awarded, UHCL 2019
- PI, Faculty Research and Support Funds (FRSF) $3,200.00, Awarded, UHCL 2018
- PI, Faculty Research and Support Funds (FRSF) $5,435.00, Awarded, UHCL 2017

- PI, NSF Travel Grant, $1580.00, Awarded 2017

Federal Research Proposals (Pending):

- NSF Fure CoRe 297455: Collaborative Research: FET: Scalable and Accelerated Quantum Circuit Simulator (PI), $204,738 ($600,000), 02/2026
- NSF SaTC2.0 297432: Collaborative Research: SaTC2.0: RES: Trusted and Secure Quantum Computing through multi-level decomposition (Co-PI), $64,986 ($600,000), 01/2026
- NSF Fure CoRe 297429: Collaborative Research: CSR: Defer-CSD: Eliminating Critical-Path Write Latency in Computational Storage for Long-Context LLM Inference (Co-PI), $173,643 ($600,000), 02/2025
- NSF DMREF 2523186, Additive Manufacturing of Advanced Composite Materials Enhanced by Machine Learning/Artificial Intelligence to Revolutionize and Engineer our Future (Co-PI), $1,628,014, 02/2025
- NSF RITEL 2603598: Collaborative Research: Transforming Integrated Circuit Education From Design to Deployment (PI), $359,995 ($900,000)

Awards:

- *Presidents Distinguished Faculty Research Award*, UHCL 2025
- *Distinguished Professorship Award*, CSE UHCL 2025
- *Minnie Stevens Piper Teaching Award (Semi-finalist Nominee*, UHCL 2025
- Hawk Spirit Award (Nominee), UHCL 2025
- Improving the Academy Award (Nominee), UHCL 2025
- DOE/LBNL Summer Research Fellowship, LBNL 2024
- Minnie Stevens Piper Award (Nominee), UHCL 2024
- DOE/LBNL Summer Research Fellowship, LBNL 2023
- Best Paper Award, IEEE UEMCON, New York, NY 2023
- DOE/LBNL Summer Research SRP VFP, LBNL 2022
- Presidents Distinguished Faculty Award in Teaching (Nominee), UHCL 2022
- Instructional Innovation Award, UHCL 2021–2022
- New Faculty Research Award (Nominee), UHCL 2021
- Minnie Stevens Piper Award (Nominee), UHCL 2018
- Best Poster Award, DataCom, Orlando, FL 2017
- Best Ph.D Forum Paper Award, IEEE ISVLSI, Tampa, FL 2014
- Dissertation Year Fellowship, FIU 2015 – 2016
- Teaching/Research Assistant Scholarship, FIU 2012-2015
- Graduate Student Appreciation Week (GSAW) Scholarship, FIU 2016
- SGA Graduate Scholarship, FIU 2015
- Graduate Student Travel Grant (GPSC), DAC2016, FIU 2016
- Graduate Student Travel Grant (GPSC), ISVLSI2014, FIU 2014
- Graduate Student Travel Grant (GPSC), SSST2013, FIU 2013
- Presidential Fellowship (Nominee), FIU 2012
- Chair, Social Planning Dept., FIU China Alumni Association 2009-Present
- Outstanding Graduate Representative (2/120), Beihang University 2007
- Outstanding Student Leader (14/500), Beihang University 2006-2007
- Student President (1/65) of Beihang–FIU IC Program 2005-2007

Industrial Certificates & Training:

- UVM Methodology Training, **AMD** 2012
- IP/SoC Tree Working Environment Training, **AMD** 2012
- dj/dv/perl/C++ Verification Environment Training, **AMD** 2012
- System Verilog and UVM Training, **Mentor Graphic** 2011
- Low-Power Technology Training (CPF design flow), **Cadence** 2011
- Assertion Training, **Synopsys** 2011
- ARM Technical Training Course, 12th to 13th October, **ARM** 2010
- Mixed-Signal Technologies – AMS tool introduction, **Cadence** 2010
- Constraint-Random Test and Coverage Training, **Synopsys** 2009
- VMM Verification Methodology, **Synopsys** 2009
- DesignWare IP Integration Training (USB2.0 OTG Controller, Ethernet Controller), **Synopsys** 2008
- DC and Layout Training, **Mentor Graphic** 2007
- Integrated Circuit Design Flow Training, **Mentor Graphic** 2006
- EDA Tools Training, ModelSim and VIM, **Mentor Graphic** 2005

Publications (2013–Present)

Book:

1. **X. Yang**, "Integrated Circuit Design: IC Design Flow and Project-Based Learning," 1st edition. Boca Raton: CRC Press, 2024. DOI: 10.1201/9781003187080. ISBN: 978-1-032-03079-1 . 506 pages.

Patents:

1. **X. Yang** and J. Andrian, "An Advanced Bus Architecture for AES-Encrypted High-Performance Embedded Systems," US Patent, **US20170302438A1**, Oct. 19, 2017.
2. **X. Yang**. 2013."A Mixed-Signal Verification System for Sigma-Delta Filters," **CN102955871A**.
3. W. Teng, J. Sun, L. Mo, J. Zou, Y. Wu, F. Liao, and J. Zhang, **X. Yang**, Ding Li. 2013. "ethod and device for detecting frame signals of wireless local area network (WLAN) equipment," **CN102970688A**.

Released IPs:

1. John Shalf, **X. Yang***, Doru Thom Popovici, and Mario Vega, "OpenFPU: OpenSource Hardware Generators for Scientific Computing," *Advanced Computation: HPC - Design & Methods, Version 1.0, 2024. [Online]. University of Houston System and Lawrence Berkeley National Laboratory. Available:
Repository Link: https://socks.lbl.gov/mvega/chisel-fp-generators.

Journals:

1. **[ToE 2025] X. Yang***, N. Wu, and X. Zhang, "Bridging Chip Design and Machine Learning in Undergraduate Digital Systems Curriculum," *IEEE Transactions on Education (***ToE - IF: 2.274)**, Major revision, 2025.

2. [**Micromachines 2023**] Mukesh Chowdary Madineni, Mario Vega, and **X. Yang**, "Parameterizable Design on Convolutional Neuron Networks with Chisel Hardware Construction Language," *MDPI Micromachines Journal*, *(***Micromachines - IF: 3.523)**, Vol 14, No. 3, PP. 531, 2022.

3. [**ToE 2021**] **X. Yang***, "Bridging the Gap Between Academia and Industry Needs with An Open Source Platform in Teaching Digital System Design," *IEEE Transactions on Education (***ToE - IF: 2.274)**, Vol. 64, Issue 4, PP. 337-344, Nov., 2021. DOI: 10.1109/TE.2021.3050450.

4. [**JSC 2021**] I. Westby and **X. Yang***, "FPGA Acceleration on a Multi-layer Perceptron Neural Network for Digit Recognition," *The Journal of Supercomputing, Springer (***JSC - IF: 2.469)**, PP. 1-18, May, 2021. DOI: 10.1007/S11227-021-03849-7

5. [**JCSC 2021**] **X. Yang*** and S. Shi, "Exploiting Energy-Quality (E-Q) Tradeoffs on Approximate FPGA Designs of Scalable Sequential Circuits," *Journal of Circuits, Systems and Computers (***JCSC - IF: 0.595)**, Vol. 30, Issue 04, Article No. 2150062, Aug. 2021. DOI: 10.1142/S0218126621500626

6. [**NNW 2020**] H. He, **X. Yang***, et. al, "Iterated Dilated Convolutional Neural Networks for Word Segmentation," *Neural Network World (***NNW - IF: 0.957)**, Vol. 30, No. 5, PP. 333-346, Oct. 2020. DOI: 10.14311/NNW.2020.30.022

7. [**IET-CDT 2020**] **X. Yang***, S. Sha, I. Unwala, and J. Lu, "Towards Third-Part IP Integration: A Case Study of High-Throughput and Low-Cost Wrapper Design on A Novel IBUS Protocol," *IET Computers & Digital Techniques (***IET-CDT - IF: 0.857)**, Vol. 14, No. 6, PP. 353-362, Nov., 2020. DOI: https://doi.org/10.1049/iet-cdt.2019.0090

8. [**TODAES 2019**] S. Sha, A. S. Bankar, **X. Yang**, W. Wen, and G. Quan, "On Fundamental Principles for Thermal-Aware Design on Periodic Real-Time Multi-Core Systems," *ACM Transactions on Design Automation of Electronic Systems (***TODAES - IF: 0.924)**, Vol. 25, No. 2, Feb. 2020. DOI: https://doi.org/10.1145/3378063

9. [**JoC 2019**] **X. Yang***, et. al., "A Vision of Fog Systems with Integrating FPGAs and BLE Mesh Network," *Journal of Communications (JoC)*, Vol. 14, No. 3, PP. 210-215, March 2019.

10. [**JETC 2018**] **X. Yang***, W. Wen, and M. Fan, "Improving AES Core Performance via An Advanced IBUS Protocol," *ACM Journal on Emerging Technologies in Computing* **(JETC - IF: 2.055)**, Vol. 14, No. 1, PP. 1-23 , March 2018. DOI: 10.1145/3110713

11. [**IJCA 2018**] Y. Zhang, **X. Yang***, etc., "Hierarchical Synthesis of Approximate Multiplier Design for Field-Programmable Gate Arrays (FPGA)-CSRmesh System," *Intl. Journal of Compt. Applications (IJCA)*, Vol. 180, No. 17 PP. 1-7, Feb. 2018

12. [**VLSID 2017**] **X. Yang***, N. Wu, and J. Andrian, "Comparative Power Analysis of An Adaptive Bus Encoding Method on The MBUS Structure," *Journal of VLSI Design (***VLSID)**, Vol. 2017, No. 4914301, PP. 1-7, May 2017.
DOI: https://doi.org/10.1155/2017/4914301

13. [**JSS 2017**] M. Fan, Q. Han, and **X. Yang**, "Energy Minimization for On-Line Real-Time Scheduling with Reliability Awareness," *Elsevier Journal of Systems and Software. (***JSS - IF: 2.559)**, Vol. 127, PP. 168-176, May 2017.
DOI: https://doi.org/10.1016/j.jss.2017.02.004

14. [**IJCA 2017**] J. Thota, P. Vangali, and **X. Yang***, "Prototyping An Autonomous Eye-Controlled System (AECS) Using Raspberry-Pi on Wheelchairs," *Intl. Journal of Compt. Applications (IJCA)*, Vol. 158, Issue 8, PP. 1-7, Jan. 2017.

15. [**CAE 2017**] P. Vangali and **X. Yang***, "A Compression Algorithm Design and Simulation for Processing Large Volumes of Data from Wireless Sensor Networks," *Communications on Applied Electronics (CAE)*, Vol. 7, Issue 4, PP. 1-5, June 2017.

16. [**Integration 2016**] **X. Yang***, N. Wu, and J. Andrian, "A Novel Bus Transfer Mode: Block Transfer and A Performance Evaluation Methodology," *Elsevier, Integration, the VLSI Journal* **Integration - IF: 1.15)**, Vol. 52, Issue: C, PP. 23-33, Jan. 2016.

17. [**IJDKP 2016**] K. Zeng, N. Wu, **X. Yang**, and K. K. Yen, "FHCC: A Soft Hierarchical Clustering Approach For Collaborative Filtering Recommendation," *Intl. Journal of Data Mining & Knowledge Management Process (IJDKP)*, Vol.6, No.3, May 2016.

18. [**TVLSI 2015**] **X. Yang*** and J. Andrian, "A High Performance On-Chip Bus (MSBUS) Design and Verification," *IEEE Transactions Very Large Scale Integr. (VLSI) Syst. (***TVLSI - IF: 1.946**), Vol. 23, Issue: 7, PP. 1350-1354, July 2015.

Conferences:

1. [**IPOPS 2026**] Doru Thom Popovici, Mario Vega, Angelos Ioannou, Fabien Chaix, Dania Mosuli, Blair Reasoner, Tan Nguyen, **Xiaokun Yang**, John Shalf, "Accelerating Density Functional Theory Calculations Through Hardware Codesign" 60th IEEE International Parallel & Distributed Processing Symposium (IPOPS) , submitted, 2026.

2. [**FPGA 2026**] Doru Thom Popovici, Mario Vega, Angelos Ioannou, Fabien Chaix, Dania Mosuli, Blair Reasoner, Tan Nguyen, **Xiaokun Yang**, John Shalf, "A Hierarchical Methodology for Hardware Design Comparison in HPC Workloads", 34th ACM/SIGDA International Symposium on Field-Programmable Gate Arrays (FPGA) , submitted, 2026.

3. [**ICDM-REU 2025**] Spencer M. Buchanan, Jose Ramos, Cameron D. Disomma, Yunxiang Zhang, Yunfeng Zhao, and **Xiaokun Yang**, "Parameterized Hardware Generation for Mini-Float Summation-of-Absolute-Differences for CNN Models" IEEE International Conference on Data Mining (ICDM) , submitted, 2025.

4. [**ICDM-REU 2025**] Jeremy W. Turner, Cameron D. Disomma, Lei Fan, Xuechen Zhang, and**Xiaokun Yang**, "Hardware Generators for Quantum Gate Emulation and Acceleration" IEEE International Conference on Data Mining (ICDM) , submitted, 2025.

5. [**ICDM-REU 2025**] Keenan Powell, Rubayet Rongon, **Xiaokun Yang**, and Xuechen Zhang, "Accelerating Deep-Learning Applications with Efficient Tensor Layout Management", IEEE International Conference on Data Mining (ICDM) , submitted, 2025.

6. [**ICDM 2025**] K. Sanchez, R. Rongon, A. Farooqui, T. E. Haynes, **Xiaokun Yang**, K. Wu, H. Tang, and X. Zhang, "Scaling Data Augmentation for Machine Learning Applications using Computational Storage Devices" IEEE International Conference on Data Mining (ICDM) , submitted, 2025.

7. [**SEET 2025**] C. D. Disomma, D. S. Musuli, and **Xiaokun Yang**, "A Reusable Software-Hardware Co-Design FPGA Platform for Floating-point Operations," 2025 The International Conference on Software Engineering of Emerging Technologies (SEET 2025), Submitted, Long Beach, CA, USA, August 11-12, 2025.

8. [**SEET 2025**] A. Cruz and **Xiaokun Yang**, "AI-Powered Engine Component Identifier for Vehicle Maintenance," 2025 The International Conference on Software Engineering of Emerging Technologies (SEET 2025), Submitted, Long Beach, CA, USA, August 11-12, 2025.

9. [**AIIoT 2025**] Brandon Fong, Nansong Wu, **Xiaokun Yang**, and Kaiman Zeng, "FPGA-Based Automatic Music Transcription as a Web Service," 2025 IEEE World AI IoT Congress (AIIoT), Accepted, Dec 2025, Osaka, Japan.

10. [**BigData 2024**] Paul Wong, Dania Susanne Mosuli, Xuechen Zhang, and **Xiaokun Yang**, "Hardware Generation on Trigonometric Functions," 2024 IEEE Big Data, DC, USA, 2024, pp. 7571-7576, doi: 10.1109/BigData62323.2024.10825243.

11. [**HPEC 2023**] Mario Vega, **X. Yang**, John Shalf, and Doru Adrian Thom Popovici, "Towards a Flexible Hardware Implementation for Mixed-Radix Fourier Transforms," 2023 IEEE High Performance Extreme Computing Conference (HPEC), Boston, MA, USA, 2023, pp. 1-7, doi: 10.1109/HPEC58863.2023.10363540.

12. [**UEMCON 2023**] C. Hingu, X. Fu, R. Challoo, J. Lu, X. Yang and L. Qingge, "Accelerating FPGA Implementation of Neural Network Controllers via 32-bit Fixed-Point Design for Real-Time Control," 2023 IEEE 14th Annual Ubiquitous Computing, Electronics & Mobile Communication Conference (UEMCON), *(***Best Paper Award**, New York, NY, USA, 2023, pp. 0445-0450, doi: 10.1109/UEMCON59035.2023.10316098.

13. [**CLOUD 2022**] G. Ding, Z. Li, Y. Wu, **X. Yang**, M. Aliasgari, and H. Xu, "Towards an Efficient Client Selection System for Federated Learning," In: Ye, K., Zhang, LJ. (eds) Cloud Computing (CLOUD 2022). Lecture Notes in Computer Science, Vol. 13731. Springer, Cham.

14. [**DAC 2022**] S. Sha and **X. Yang**, "Endurance Aware Real Time Scheduling on ReRAM Accelerators," IEEE/ACM 2022 Design Automation Conference *(***DAC 2022)**, WIP, Moscone West, San Francisco, USA, 2022.

15. [**ISQED 2022**] A. L. Reed and **X. Yang**, "Lightweight Neural Network Architectures for Resource-Limited Devices," IEEE/ACM 23rd International Symposium on Quality Electronic Design *(***ISQED 2022, Acceptance Rate: 30%)**, PP. 1-7, Santa Clara, CA, USA, 2022.

16. [**ISMCR 2022**] M. Vega, M. Madineni, and **X. Yang**, "Case Studies of Configurable Binary Design Library on FPGA," IEEE 23rd International Symposium on Measurement and Control in Robotics (ISMCR 2022), PP. 1-5, Houston, TX, USA, 2022.

17. [**ISMCR 2022**] S. K. Surapally, and **X. Yang**, "Evaluating FPGA Acceleration on Binarized Neural Networks and Quantized Neural Networks," IEEE 23rd International Symposium on Measurement and Control in Robotics (ISMCR 2022), PP. 1-5, Houston, TX, USA, 2022.

18. [**GreenTech 2022**] M. Ejaz, I. Unwala, J. Lu, and **X. Yang**, "Securing Hardware Development Process using Blockchain," 2022 IEEE Green Technologies Conference (GreenTech), PP. 150-153, Houston, TX, USA, 2022.

19. [**CSCE 2021**] S. Ek, M. Curci, **X. Yang**, et. al, "Sentiment Analysis of Long-term Social Data during the COVID-19 Pandemic," The 2020 World Congress in Computer Science, Computer Engineering, and Applied Computing (CSCE 2020), Las Vegas, 2021.

20. [**ICAI 2021**] I. Westby, H. Koc, J. Lu, and **X. Yang***, "A Design on Multilayer Perceptron (MLP) Neural Network for Digit Recognition," PP. 729-741, Advances in Artificial Intelligence and Applied Cognitive Computing. Transactions on Computational Science and Computational Intelligence. Springer, Cham. 2020.
DOI: https://doi.org/10.1007/978-3-030-70296-0_53

21. [**ICAI 2021**] A. Gajjar, S. Dave, T. Andrew Yang, L. Wu, and **X. Yang***, "An IoT-Edge-Server System with BLE Mesh Network, LBPH, and Deep Metric Learning," PP. 757-773, Advances in Artificial Intelligence and Applied Cognitive Computing. Transactions on Computational Science and Computational Intelligence. Springer, Cham. 2021. https://doi.org/10.1007/978-3-030-70296-0_55

22. [**ICAI 2021**] **X. Yang***, T. Andrew Yang, and L. Wu, "An Edge Detection IP of Low-cost System-on-Chip for Autonomous Vehicles," PP. 775-786, Advances in Artificial Intelligence and Applied Cognitive Computing. Transactions on Computational Science and Computational Intelligence. Springer, Cham. 2021.
DOI: https://doi.org/10.1007/978-3-030-70296-0_56

23. [**CSCE 2021**] L. Wu, A. Yang, A. Dubrovskiy, H. He, H. Yan, **X. Yang**, et. al, "Advancing AI-aided Computational Thinking in STEAM (Science, Technology, Engineering, Arts, Math) Education (Act-STEAM)," PP. 787-795, Advances in Artificial Intelligence and Applied Cognitive Computing. Transactions on Computational Science and Computational Intelligence. Springer, Cham. 2020.
DOI: https://doi.org/10.1007/978-3-030-70296-0_57

24. [**CSCE 2021**] L. Wu, A. Yang, H. Yan, **X. Yang**, et. al, "Realistic Drawing & Painting with AI Supported Geometrical and Computational Method (Fun-Joy)," PP. 797-804, Advances in Artificial Intelligence and Applied Cognitive Computing. Transactions on Computational Science and Computational Intelligence. Springer, Cham. 2020. DOI: https://doi.org/10.1007/978-3-030-70296-0_58

25. [**ISQED 2019**] **X. Yang***, Y. Zhang, and L. Wu,"A Scalable Image/Video Processing Platform with Open Source Design and Verification Environment," 20th Intl. Symposium on Quality Electronic Design *(***ISQED 2019, Acceptance Rate: 35%)**, PP. 110-116, Santa Clara, CA, USA, 2019.

26. [**ISVLSI 2019**] Vaca, K., A. Gajjar, and **X. Yang***, "Real-Time Automatic Music Transcription (AMT) with Zync FPGA," 2019 IEEE Computer Society Annual Symposium on VLSI *(***ISVLSI 2019, Acceptance Rate: 17%)**, PP. 378-384, Miami, FL, USA, 2019.

27. [**ISVLSI 2019**] Zhang Y., **X. Yang***, "A Case Study On Approximate FPGA Design With an Open-Source Image Processing Platform" 2019 IEEE Computer Society Annual Symposium on VLSI *(***ISVLSI 2019, Acceptance Rate: 17%)**, PP.372-377, Miami, FL, US, 2019.

28. [**ISMCR 2019**] K. Vaca, M. Jefferies, and **X. Yang***, "An Open Real-Time Audio Processing Platform on Zync FPGA," Intl. Symposium on Measurement and Control in Robotics (ISMCR 2019), PP. D1-2-1-D1-2-6, Houston, TX, USA, 2019.

29. [**ISMCR 2019**] X. Zhang, J. Lu, X. Fu, **X. Yang**, I. Unwala, and T. Zhang, "Tracking of Targets in Mobile Robots Based on Camshift algorithm," Intl. Symposium on Measurement and Control in Robotics (ISMCR 2019), PP. B2-3-1-B2-3-5., UHCL, Houston, USA, Sept 19-21, 2019.

30. [**ICAI 2019**] H. He, L. Wu, H. Yan, and **X. Yang**, "Synthesize Corpus for Chinese Word Segmentation," The 21st Intl. Conference on Artificial Intelligence (ICAI 2019), PP.129-134, Las Vegas, NV, USA, 2019.

31. [**HONET-ICT 2019**] J. Gopaluni, I. Unwala, J. Lu, and **X. Yang**, "Graphical User Interface for OpenThread," 2019 IEEE 16th Intl. Conference on Smart Cities: Improving Quality of Life Using ICT & IoT and AI (HONET-ICT 2019), PP. 235-237, Charlotte NC, USA, Oct. 6-9, 2019.

32. [**CSE 2019**] X. Fu, J. Lu, X. Zhang, **X. Yang**, and I. Unwala, "Intelligent in-vehicle safety and security monitoring system with face recognition," 2019 IEEE Intl. Conference on Computational Science and Engineering (CSE 2019), PP. 225-229, New York, NY, USA, Dec. 05 2019, 2019.

33. [**Dual 2019**] Isaac Westby and **X. Yang***, "Real-time Digit Recognition with Neural Network on a Video Processing FPGA Platform," 2018 IEEE Innovation and Automation Conference, Gilruth Recreation Center, NASA-JSA, Houston, Nov. 15, 2019.

34. [**CSCI 2018**] A. Gajjar, **X. Yang***, et.al., "Mesh-IoT Based System For Large-Scale Environment," 5th Annual Conf. on Computational Science & Computational Intelligence (CSCI 2018), PP. 1019-1023, Las Vegas, NV, USA, 2018.

35. [**CSCI 2018**] J. Gopaluni, I. Unwala, J. Lu, and X. Yang , "Implementation of GUI for OpenThread," 5th Annual Conf. on Computational Science & Computational Intelligence (CSCI 2018), PP. 1015-1018, Las Vegas, NV, USA, 2018.

36. [**ICACS 2018**] A. Gajjar, **X. Yang***, et. al.., "An FPGA Synthesis of Face Detection Algorithm using HAAR Classifiers," Intl. Conference on Algorithms, Computing and Systems (ICACS 2018), PP.133-137, Beijing China, July 2018.

37. [**ICACS 2018**] Y. Zhang, **X. Yang***, et. al., "Exploring Slice-Energy Saving on An Video Processing FPGA Platform with Approximate Computing" Intl. Conference on Algorithms, Compting and Systems (ICACS 2018), PP.138-143, Beijing China, July 2018.

38. [**ITNG 2018**] H. He, L. Wu, **X. Yang**, et. al., "Dual Long Short-Term Memory Networks for Sub-Character Representation Learning," The 15th Intl. Conference on Information Technology - New Generations (ITNG 2018), Springer Advances in Intelligent Systems & Computing Book Series, Springer-Verlag, Las Vegas, NV, USA, 2018.

39. [**Dual 2018**] **X. Yang***, "A Scalable Image/Video Processing Platform with FPGA Design and Verification Environment," 2018 IEEE Innovation and Automation Conference, Gilruth Recreation Center, NASA-JSA, Houston, Nov. 3, 2018.

40. [**Dual 2018**] A. Gajjar, **X. Yang***, "Mesh-IoT Based Smart and Secure System for Wide-Range Territory," 2018 IEEE Innovation and Automation Conference, Gilruth Recreation Center, NASA-JSA, Houston, Nov. 3, 2018.

41. [**DASC 2017**] L. Nwosu, H. Wang, J. Lu, I. Unwala, **X. Yang**, et. al., "Deep Convolutional Neural Network for Facial Expression Recognition Using Facial Parts," 2017 IEEE 15th Intl Conf on Dependable, Autonomic and Secure Computing (DASC 2017, Best Poster Award), PP. 1318-1321, Orlando, FL, USA, 2017.

42. [**ASP-DAC 2017**] **X. Yang*** and W. Wen, "Design of A Pre-Scheduled Data Bus (DBUS) for Advanced Encryption Standard (AES) Encrypted System-on-Chips (SoCs)," The 22nd Asia and South Pacific Design Automation Conference, **(ASP-DAC 2017 - Regular Paper, Acceptance Rate:111/358=31%)**, PP. 506-511, Chiba, Japan, Jan. 2017.

43. [**SEC 2017**] **X. Yang*** and X. He, "Establishing a BLE Mesh Network using Fabricated CSRmesh Devices," The 2nd ACM/IEEE Symposium on Edge Computing **(SEC 2017, Acceptance Rate: 40%)**, No. 34, San Jose/Fremont, CA, US, 2017.

44. [**AHFE 2017**] **X. Yang*** and N. Wu, "Design of A Bio-Feedback Digital System (BFS) Using 33-Step Training Table for Cardio Equipment," The 8th Intl. Conference on Applied Human Factors and Ergonomics (AHFE 2017), PP. 53-64, Los Angeles, California, 2017.

45. [**ICAC 2017**] **X. Yang***, Y. Zhang, W. Wen, and M. Fan, "A Case Study of Self-Organization Algorithms for High-Efficiency System-on-Chips Integration," IEEE Intl. Conf. on Autonomic Computing (ICAC 2017) – Workshop on Feedback Computing, Columbus, Ohio, US, 2017.

46. [**FYEE 2017**] N. Wu, K. Zeng, J. Weidenfeller, and **X. Yang**, "Flipping the Classroom for Enhancing Learning and Designing in an Embedded Systems Class, " The 1st Year Engineering Experience Conference (FYEE 2017) , PP.1-4, Daytona Beach, FL, 2017.

47. [**ICI 2017**] D. Wu, N. Wu, K. Zeng, and **X. Yang**, "Recognizing Unconstrained Handwritten Digit Based on Shape Analysis and Multi-class SVM Classification," The 8th Intl. Conference on Information (ICI 2017), Tokyo, Japan, May 2017.

48. [**SEC 2017**] A. Gajjar, Y. Zhang, and **X. Yang***, "A Smart Building System Integrated with An Edge Computing Algorithm and IoT Mesh Networks," The Second ACM/IEEE Symposium on Edge Computing **(SEC 2017, Acceptance Rate: 40%)**, Article No. 35, San Jose/Fremont, CA, US, 2017.

49. [**Dual 2017**] Y. Zhang and **X. Yang***, "A Novel Fog Computing Acceleration Method: Approximate FPGA Design on Adder and Multiplier," 2017 IEEE Innovation and Automation Conference, Gilruth Recreation Center, NASA-JSA, Houston, Oct. 28, 2017.

50. [**Dual 2017**] A. Gajjar and **X. Yang***, "A Wide Area IoT Mesh Network With Edge Computing," 2017 IEEE Innovation and Automation Conference, Gilruth Recreation Center, NASA-JSA, Houston, Oct. 28, 2017.

51. [**Dual 2017**] **X. Yang***, "A Prototype in Fog Computing (FC) : Design of An FPGA-CSRmesh (FC) Platform Toward Wide-Area and Low-Energy IoT Networks, ‘’ 2017 IEEE Innovation and Automation Conference, Gilruth Recreation Center, NASA-JSA, Houston, Oct. 28, 2017.

52. [**ICI 2017**] D. Wu, N. Wu, K. Zeng, and **X. Yang***, "Recognizing Unconstrained Handwritten Digit Based on Shape Analysis and Multi-class SVM Classification," The 8th Intl. Conference on Information (ICI 2017), Tokyo, Japan, May 2017.

53. [**DAC 2016**] **X. Yang*** and J. Andrian, "A Configurable and Synthesizable On-Chip Bus Architecture for Integrating Industrial Standard IPs," 2016 Design Automation Conference *(***DAC 2016)**, WIP, Austin, TX, USA, June 2016.

54. [**ISVLSI 2014**] **X. Yang*** and J. Andrian, "A Low-Cost and High-Performance Embedded System Architecture and An Evaluation Methodology," IEEE Computer Society Annual Symposium on VLSI *(***ISVLSI 2014 - Best Ph.D Forum Paper Award)**, PP. 240-243, Tampa, FL, USA, 2014.

55. [**SSST 2013**] **X. Yang*** X. Niu, and J. Fan, "Mixed-Signal System-on-Chip (SoC) Verification Based on System Verilog Model," The 45th Southeastern Symposium on System Theory (SSST 2013), PP. 17-21, Waco, TX, USA, 2013.

Abstracts/Posters, Presentations, and Invited Talks:

1. [**Quantum 26**] Xiaokun Yang, Beyond Moore's Law: Hybrid Quantum-Classical Platforms, Invited Talk, Case Western Reserve University.

2. [**Quantum 26**] Xiaokun Yang, Beyond Moore's Law: Specialized Hardware Design Generation for Quantum Circuit Simulation and Verification, Invited Talk, Quantum Workshop, UT Dallas.

3. [**SC 25**] Mario Vega, Angelos Ioannou, Fabien Chaix, Dania Mosuli, Blair Reasoner, Tan Nguyen, Xiaokun Yang, and John Shalf, "An Approach to Identify Divergences in Hardware Designs for HPC Workloads", 11th International Workshop on Heterogeneous High-Performance Reconfigurable Computing (H2RC 2025), San Luis, MO, 21 November 2025.

4. [**NSF REU Seminar 2025**] **X. Yang**, "Specialized Hardware Design on Linear Algebra for Applications in Scientific Computing, ML, and Quantum Circuit Emulation" *(***UHCL Seminar 2025)**, Vancouver, WA, July 24, 2025.

5. [**NSF REU Poster 2024**] Jeremy Turner and Xiaokun Yang, "Hardware Generation and Acceleration for Quantum Gate Simulation", Poster, ENCS Undergraduate Research Showcase, Vancouver, WA, August 14, 2025.

6. [**NSF REU Poster 2024**] Jose Ramos and Xiaokun Yang, "Code Generation for AdderNet Neural Network", Poster, ENCS Undergraduate Research Showcase, August 14, 2025.

7. [**UHCL Physics & Mechanical Seminar 2025**] **X. Yang**, "DFT Beyond Moore's Law: Hardware Acceleration for Future HPC," *(***UHCL Seminar 2025)**, February 25, 2025.

8. [**LBL Fellowship Poster 2024**] Blair Reasoner, Xiaokun Yang, Doru Thom Adrian Popovici, Patricia Gonzalez-Guerrero, Meriam Gay Bautista, Mario Vega, and John Shalf, "DFT Beyond Moore's Law: Extreme Hardware Specialization for the Future of HPC", Poster, Berkeley National Laboratory, 2024.

9. [**NSF REU Poster 2024**] Keaton Khoury, Blair Reasoner, Paul Wong, and Xiaokun Yang, "Design and Verification of Submodules for Density Functional Theory (DFT) Hardware Accelerator", Poster, Undergraduate Research Showcase, Vancouver, WA, July 30, 2024.

10. [**NSF REU Poster 2024**] Paul Wong and Xiaokun Yang, "Trigonometric Functions in the Chisel Hardware Construction Language", Poster, Undergraduate Research Showcase, Vancouver, WA, July 30, 2024.

11. [**NSF REU Seminar 2024**] **X. Yang**, "Beyond Moore's Law: Hardware Acceleration for Future HPC and ML," *(***NSF REU Seminar 2024)**, July 12, 2024.

12. [**LBL Fellowship Poster 2023**] Blair Reasoner, Xiaokun Yang, Doru Thom Adrian Popovici, Patricia Gonzalez-Guerrero, Meriam Gay Bautista, Mario Vega, and John Shalf, "Parameterized Hardware Accelerator Design on Tall-Skinny QR Factorization", Poster, Berkeley National Laboratory, 2024.

13. [**SRP 2023**] **X. Yang**, "Specialized Hardware Design on DFT for HPC," *(***DOE SRP 2023)**, January 9-13, 2023.

14. [**LBL 2022**] **X. Yang**, "DFT Beyond Moore's Law: FPGA Design Specialization for HPC," LBL Monthly Conference, *(***LBL 2022)**, Nov. 02, 2022.

15. [**DOE VFP 2022**] **X. Yang**, Mario Vega, Doru Adrian Thom Popovici, Nirmalendu Patra, and John Shalf, "DFT Beyond Moore's Law: FPGA Design Specialization for the 3D-FFT for HPC," DoE VFP Summer 2022 Oral Presentation *(***DOE VFP 2022)**, Aug. 5, 2022.

16. [**WDE 2022**] Mario Vega, **X. Yang**, Doru Adrian Thom Popovici, Nirmalendu Patra, and John Shalf, "DFT Beyond Moore's Law: Hardware Design Specialization for Streaming and Mixed FFTs," WDE Poster Presentation *(***WDE 2022)**, July 22, 2022.

17. [**CFD 2022**] **X. Yang***, "Project-Centric Learning with OpenIC," Faculty Development Week, Center for Faculty Development, UHCL, Jan. 27, 2022.

18. [**SRP 2022**] **X. Yang**, "High-Performance SoC Architecture," *(***DOE SRP 2022)**, December 9-13, 2021.

19. [**GCC 2021**] **X. Yang***, "FPGA Designs and Acceleration for Neural Networks," GCC Translational Imaging Conference, Gulf Coast Consortia for Quantitative Biomedical Science, Invited Short Talk, Virtual Event, Nov. 2, 2021.

20. [**ES 2021**] **X. Yang***, "FPGA Acceleration on Artificial Intelligence", Invited Talk, Engineering Science Department, Sonoma State University, CA, 2021.

21. [**VRISE 2021**] **X. Yang***, "An Implementation of Low-Cost System-on-Chip with Neural Network for Surveillance Cameras," TC17- VRISE2021 - Topical Event on Robotics for Risky Interventions and Environmental Surveillance, Virtual Event, ICI and IEEE Galveston Bay Section, Oct. 8, 2021.

22. [**ICAMSE 2019**] **X. Yang***, "An Advanced SoC Architecture for Low-Cost And Low-Power Edge Devices," International Conference on Advanced Materials Sciences and Engineering, Osaka, Japan, 2019

23. [**Robotics 2018**] **X. Yang***, Y. Zhang, A. Gajjar, H. Schmoyer, and N. Ly, "Learning-on-Chip: Facial Detection with Approximations of FPGA Computing," 2018 Robotics & AI Day, UHCL, Aug. 03, 2018.

24. [**Robotics 2017**] Y. Zhang and **X. Yang***, "Exploring Approximate Designs for FPGA-Based Edge Computing," 2017 Robotics & AI Day, UHCL, July 21, 2017.

25. [**Robotics 2017**] A. Gajjar and **X. Yang***, "A Smart Building System Integrated with An Edge Computing Algorithm and IoT Mesh Networks," 2017 Robotics & AI Day, UHCL, July 21, 2017.

26. [**GBS 2016**] **X. Yang***, "A High Performance Advanced Encryption Standard (AES)-Encrypted On-Chip Bus Architecture for Internet-of-Things (IoT) System-on-Chips (SoCs)," IEEE Galveston Session, NASA-JSA, Gilruth Recreation Center, Nov. 17, 2016.

Research Activities

Membership:

- IEEE Member 2013–
- IEEE Galveston Bay Section Member 2017–
- TC on VLSI (TCVLSI) 2020–
- TC on Electronic Design Automation (CEDA) 2020–
- ACM Member 2016–
- SIG in Artificial Intelligence (SIGAI) 2020–
- IACSIT Senior Member 2018–

Editorial Board, Associate Editor, and Publication Chair:

- Guest Editor, MDPI Micromachines Journal, Special Issue "Beyond Moore's Law: Hardware Specialization and Advanced System on Chip" 2022-2023.
- Associate Editor/Track Chair, Symposium/Workshop - Hardware Acceleration on AI, Intl. Conference on Artificial Intelligence (ICAI 2020), July 2020.
- Publication Chair: 2019 2nd Intl. Conference on Algorithms, Computing and Artificial Intelligence (ACAI 2019), Sanya, China, Dec., 2019

Book/Book Proposal Reviewer:

- CRC Press Book proposal - The Thermal-Constrained Real-Time Scheduling on Multi-Core Platforms-An Analytical Approach 2019
- CRC Press Book: Empowering the High-Performance Computing by Process-in-Memory on 3D Processors 2019

Journal Reviewer:

- Microprocessors and Microsystems Journal 2024
- Journal of Circuits, Systems, and Computers 2024
- IEEE Transactions on Green Communications and Networking (TGCN) 2021
- Elsevier, Sustainable Computing, Informatics and Systems (SUSCOM) 2019, 2020, 2021
- Elsevier, Integration, the VLSI Journal (VLSI) 2017, 2019, 2021
- Elsevier, Automation in Construction 2022
- Elsevier, Knowledge-Based System 2021, 2022-1, 2022-2
- Springer, The Journal of Supercomputing 2020, 2021-1, 2021-2, 2022
- Springer, SN Computer Science 2020
- Springer, Journal of Real-Time Image Processing (RTIP) 2020
- Taylor & Francis, Cogent Engineering 2021
- Taylor & Francis, Imaging Science Journal, 2022
- MDPI, Journal of Low Power Electronics and Applications 2021
- IEEE Trans. on VLSI Syst. (TVLSI) 2015, 2017, 2019

- IEEE Trans. on Education (ToE) 2019
- IEEE Trans. on Industrial Informatics (TII) 2018
- IET Computer & Digital Techniques (IET-CDT) 2017-1, 2017-2, 2019, 2020

Organizer/Section Chair:

- 2025 25th IEEE International Conference on Data Mining (IEEE ICDM), Washington DC, USA, November 12-15, 2025.
- 2024 IEEE International Conference on Big Data (BigData), Washington, DC, USA, 2024.
- IEEE 17th Intl. Conf. on Smart Communities (HONET2020), Charlotte, NC, Dec. 14-16, 2020.
- IEEE Computer Society Annual Symposium on VLSI (ISVLSI 2019) - Circuit, Reliability and Fault Tolerance II, Miami, FL, US, July, 2019.
- IEEE Innovation and Automation Conference - IoT Section, Guilruth ctr., NASA, Oct., 2017.
- Intl. Conference on Microelectronic Devices and Technologies (MicDAT), 2021, 2020, 2019, 2018.
- IEEE Symposium on Internet of Things & Internet of Everything in the 5th Annual Conf. on Computational Science & Computational Intelligence (CSCI2018), Las Vegas, Nevada, USA, Dec., 2018.

TPC & Conference Reviewer :

- IEEE Intl. Conference on Smart Communities: Improving Quality of Life Using ICT, IoT and AI (HONET), 2021, 2020, 2019
- BenchCouncil Intl. Symposium on Benchmarking, Measuring and Optimizing (Bench), 2021
- IEEE Computer Society Annual Symposium on VLSI (ISVLSI), 2019
- IEEE Intl. Symposium on Measurement and Control in Robotics (ISMCR), 2019
- IEEE Intl. Conference on Communication and Information Systems (ICCIS), 2019
- ACM The World Symposium on Software Engineering (WSSE), 2019
- IEEE Intl. Conference on Computing, Networking and Communications (ICNC), 2019
- IEEE Intl. Conference on Communication and Information Systems (ICCIS), 2019, 2018
- ACM Intl. Conference on Algorithms, Computing, and Systems (ICACS), 2018
- ACM Intl. Workshop on Computer Science and Engineering (WCSE), 2019, 2018
- IEEE/ACM Intl. Symposium on Nanoscale Architectures (Nanoarch), 2017, 2015
- IEEE International Conference on Distributed Computing Systems (ICDCS), 2019
- Intl. Conference on Sustainable Computing in Science, Technology & Management (SUSCOM), 2019
- IEEE Intl. Symposium on Quality Electronic Design (ISQED), 2016
- IEEE Intl. Conference on Network, Architecture and Storage (NAS), 2016

University Services:

- CENG Asst. Professor Search Committee 2024, 2025
- CENG Lecturer Search Committee 2021
- CENG ABET Committee 2017 –
- CENG Graduate Admission Committee 2022 –
- CENG Undergraduate Assessment 2021 –

- CENG Advisory Board Meetings 2017 –
- CENG Senior Project Final Presentations Chair and Organizer 2019 –
- CSE Orientations for new students 2017 –
- CSE Orientations for new international students 2017 –
- CSE Fall and Spring Graduate Advising and Registration Events 2016 –
- Presenter, UHCL - Faculty Development Week Presentations, 2022
- UHCL Student Affairs Committee 2018 –
- UHCL Commencement Ceremonies 2017 –
- UHCL Discover 2019 –
- UHCL University Open Houses 2016 –
- UHCL Graduate Preview 2019 –
- UHCL Hawk Premier 2016 –
- UHCL Orientations for new students 2017 –
- UHCL Orientation for new international students 2017 –
- Presenter, UHCL - IEEE Student Branch Professor's Day 2016
- Presenter, UHCL - Robotics & AI Day 2017, 2018

Community Services:

- Judge, 2022-23 Clear Creek ISD Science and Engineering Fair 2022
- Executive Committee, IEEE Galveston Bay Section, Houston, TX 2021
- Collaboration with and mentorship of students at Sonoma State University, CA 2020-present
- Presenter, ES lecture series in the Engineering Science Department, Sonoma State University, CA 2021
- Academic program external reviewer, Auburn University at Montgomery, AL 2020-present
- Proposal external reviewer, Wilkes University PA, 2020
- Judge, 61st CCISD Elementary Science & Engineering Fair 2020
- Judge, CCISD Junior and Senior Science Fair 2020
- Judge, Science & Engineering Fair of Houston 2019, 2020
- Presenter, IEEE Galveston Session Monthly Meeting 2017
- Session Chair, IEEE Galveston Session Conference 2017
- GSAW Scholarly Forum, Oral Presenter March 2016
- 2015 Miami Maker Fair, IoT Device Exhibitor Feb. 2015
- 2014 Hongkong Electronics Fair (Autumn Edition), IoT Device Exhibitor Spet. 2015
- IEEE Workshop – Industrial Standard Integrated Circuit Design Flow, Invited Talk Aug. 2013

Teaching Experience

Associate Professor – UHCL: 2016 – Present

- Master's Thesis (CENG 6939)
- Research Project and Seminar (CENG 6838)
- Integrated Circuit Design Flow (CENG 5931/4931)
- Graduate Independent Study (CENG 5919)
- Advanced Digital System Design (CENG5534)
- Undergraduate Independent Study (CENG 4389)

- Digital System Design (CENG4354)
- Senior Project I&II (CENG4265&CENG4266)
- Electronics (CENG3316)
- Lab for Computer Architecture (CENG3151)
- Lab for Electronics (CENG3116)
- Lab for Linear Circuit (CENG2113)
- Lab for Digital Circuit (CENG2112)

Industry Experience

ASIC/SoC Design/Tape-out Experiences:

- AMD – Sr. IC Design & Verification Engineer 2011-2012
  - a. AMD Assertion Tool Development and Testing
  - b. UVM Verification Methodology
  - c. USB3.0, PCIE Design and Research
  - d. Low Power Design and Verification, Clock Gate and Power Domain Description
  - e. IP Design and Verification: I2C/SPI/GPIO/SDIO/UART/Flash/Smart Card/IR/Interrupt handler/Semaphore, etc.
  - f. Design and Verification: DMA and DDRC
- CEC HED Corp. – Sr. IC Verification Engineer 2009-2010
  - a. 802.11a/b/g/n System Level Verification
    - a.1 UVM Methodology and RGM (Register and Memory Package)
    - a.2 Low Power Design
    - a.3 Mix-Signal Verification with RVM (Real Valued Modeling).
    - a.4 DA, DeMux, Delta Sigma Modulator Design
  - b. 802.11a/b/g/n BBP (Base Band) Verification
    - b.1 Constraint Random, Function & Code Coverage, Assertion Design
    - b.2 Transmitting, Receiving, and Signal Channel Model Integration
    - b.3 RF Models Design by RVM: LNA, Mixer, VGA, AD, PA and DA
- PowerLayer MicroSystems Corp. (PLM) – IC Design Engineer 2007-2008
  - a. USB 2.0 OTG Integration and Verification
    - a.1 USB2.0 Host, Synopsys Nano-PHY and VIP Integration and Verification
    - a.2 USB2.0 and UTMI+ Integration
  - b. Ethernet, Synopsys MII/RMII PHY Integration and Verification
    - b.1 10/100 Mbps Data, Full-Duplex and IEEE 802.3x Support
    - b.2 Soc Bus Integration and Verification.
  - c. PLM3K Circuit System Level Verification
    - c.1 V3K CPU Design and Verificaiton
    - c.2 SoC Peripherals: I2C, SPI, GPIO, SDIO, UART, Flash Controller, Smart Card Controller, IR Controller, etc.
    - c.3 Post Processing Verification: TNR, SNR, SCALER, SE Plane, etc.

Methodologies, Languages, and EDA Tools:

- Professional in industry ASIC/FPGA/SoC design flow
- Professional in hardware description language: Verilog and VHDL
- Professional in hardware verification language: System Verilog
- Professional in design flow scripts: dj, dv, tcl, cshell, Makefile, perl
- Professional in verification methods: ADV, CDV, CRV

- Professional in UNIX/LINUX and EDA tools: Vim; Debussy/Verdi; ModelSim/Questa, NC, VCS, Quasta; DC, PT and so on.
- Professional in FPGA tools: Xilinx ISE/Vivado, Intel Quartus
- Professional in verification methodology – VMM and UVM
- Professional in low power design methods: clock gate and power domain design methods (CPF and UPF)
- Familiar with mix-signal verification methods: SPICE, AMS, RVM

Industrial Specifications:

- Professional in SoC architectures: AMBA APB, AHB, AXI, OCP, Wishbone.
- Professional in SoC controllers: ARM/MIPS, DMA, DDR2 Controller.
- Professional in security protocols: AES and DES.
- Professional in interface specifications: USB2.0 OTG – Nano-PHY, VIP, UTMI+; IEEE 802.3x Ethernet – MII/RMII Phy; PCIE; Infrared Remote.
- Professional in Wireless communication Protocols: Wi-Fi 802.11a/b/g/n Baseband, Bluetooth 4.0 (LE).
- Professional in SoC peripherals: Interrupt Controller, Semaphore, UART, I2C, SPI, SDIO, GPIO, WatchDog, Timer, and so on.
- Professional in memory controllers: Smart Card, NAND/NOR/Serial Flash, E2ROM.
- Familiar with graphic modules: TNR, SNR, SCALER, SE, Pre-Processing, Post-Processing.
- Familiar with mix-signal model design: DA, DeMux, Delta Sigma Modulator, LNA, Mixer, VGA, AD, PA, and DA.